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Analytical modeling of metal gate granularity based threshold voltage variability in NWFET

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ABSTRACT

Estimation of threshold voltage V_T variability for NWFETs has been computationally expensive due to lack of analytical models. Variability estimation of NWFET is essential to design the next generation logic circuits. Compared to any other process induced variabilities, Metal Gate Granularity (MGG) is of paramount importance due to its large impact on V_T variability. Here, an analytical model is proposed to estimate V_T variability caused by MGG. We extend our earlier FinFET based MGG model to a cylindrical NWFET by satisfying three additional requirements. First, the gate dielectric layer is replaced by Silicon of electro-statically equivalent thickness using long cylinder approximation; Second, metal grains in NWFETs satisfy periodic boundary condition in azimuthal direction; Third, electrostatics is analytically solved in cylindrical polar coordinates with gate boundary condition defined by MGG. We show that quantum effects only shift the mean of the V_T distribution without significant impact on the variability estimated by our electrostatics-based model. The V_T distribution estimated by our model matches TCAD simulations. The model quantitatively captures grain size dependence with $\sigma(V_T)$ with excellent accuracy (6%error) compared to stochastic 3D TCAD simulations, which is a significant improvement over the state-of- the-art model with fails to produce even a qualitative agreement. The proposed model is 63× faster compared to commercial TCAD simulations.

1. Introduction

NWFET (Nanowire Field Effect Transistor) has emerged as the potential replacement for FinFET as an ultimate scaled CMOS device [1]. For both FinFET and NWFET, process induced variabilities have been very challenging from circuit performance viewpoint. Multi-gate transistors exhibit higher Metal Gate Granularity (MGG) variability compared other variability phenomena like Line Edge Roughness (LER), Random Dopant Fluctuation (RDF) etc. [2–5]. The wider the V_T distribution, the worse is the circuit performance [6]. Hence, the estimation of V_T distribution is a must before circuit design.

It was reported that the NWFET (gate all around nanowire MOSFET) has better immunity against MGG induced variability compared to that of FinFET by 3D TCAD simulations in [7]. The smaller V_T variability in NWFET is a strong motivation to replace FinFET with NWFET in future technology nodes. The steep computation cost of 3D stochastic TCAD simulations to extract variability seeks for more computationally efficient techniques. The V_T distribution from smaller grain sizes typically result in a Gaussian like distribution while the larger grains produce a bimodal distribution (in case of two WF values). Any analytical method or model should be able to capture this size dependence efficiently. Further, analytical models are intuitive, faster than TCAD and can be a stepping-stone to a compact model. Recently, our group has developed the analytical estimation of the V_T variability in FinFETs [8].

In this work, we extend the FinFET based MGG model to NWFET with cylindrical geometry by satisfying three additional constraints. The results from this model agree well with TCAD. Quantum confinement (not accounted in our model) produces a shift in the V_T distribution without affecting its shape. The model is compared to state-of-the-art to show significant improvement achieved.

2. The analytical model

The body potential of NWFET is analytically modeled in [9,10]. Due to very low free carrier concentration in sub-threshold regime, the electrostatics of the NWFET can be captured by the Laplace equation alone instead of Poisson equation [9]. A 3D schematic of the NWFET with MGG is shown in Fig. 1(a). A simple cylinder is assumed for the purpose of solving the Laplace equation. Two flat faces (planes) of the cylinder correspond to two boundary conditions (Source and the Drain) and the curved surface of the cylinder corresponds to the third boundary condition i.e. the Gate. The thin gate dielectric is substituted

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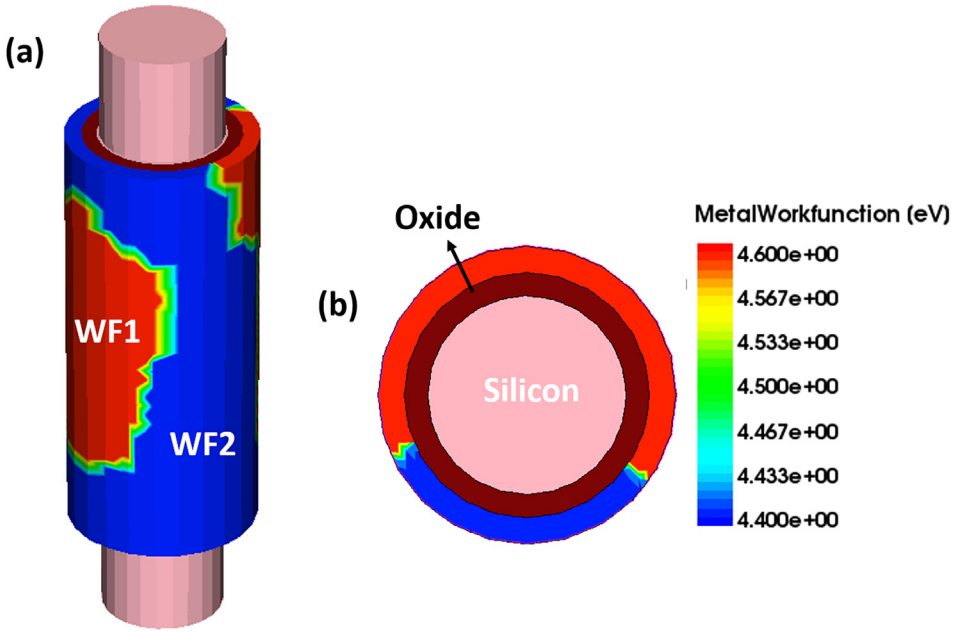

Fig. 1. (a) Structure of the NWFET with MGG which constitutes two distinct work-function on the Gate. The red and blue regions show two types of work functions (b) Cross-sectional view of the NWFET with gate metal, Silicon (channel) and oxide. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

with electro-statically equivalent, thicker Silicon to form a single homogeneous cylinder. This simplification is essential for obtaining a closed form expression for the electrostatic potential. Due to this, the radius gets modified to effective (new) radius (t_{si}) and is given by (1).

$$t_{si} = r \times e^{\frac{\epsilon_{si}}{\epsilon_{ox}} \ln\left(\frac{r+t_{ox}}{r}\right)} = r\eta \tag{1}$$

where $r\left(=\frac{d}{2}\right)$ is the radius of the nanowire, d is the diameter, ϵ_{si} and ϵ_{ox} are the relative permittivities of the Silicon and the Oxide. The Gate length (L_g) remains unchanged. Due to this transformation, the actual grain gets stretched out only in the horizontal direction (azimuthal direction) by the factor η as given by (1). This grain distortion is illustrated in Fig. 2. The procedure of finding variability in V_T distribution is presented in three consecutive subsections below.

2.1. Cylindrical gate MGG generation

In this section, the algorithm for generating random metal gate grains is presented. This is similar to the algorithm used for FinFET in [8] except a grain periodicity constraint in the azimuthal direction.

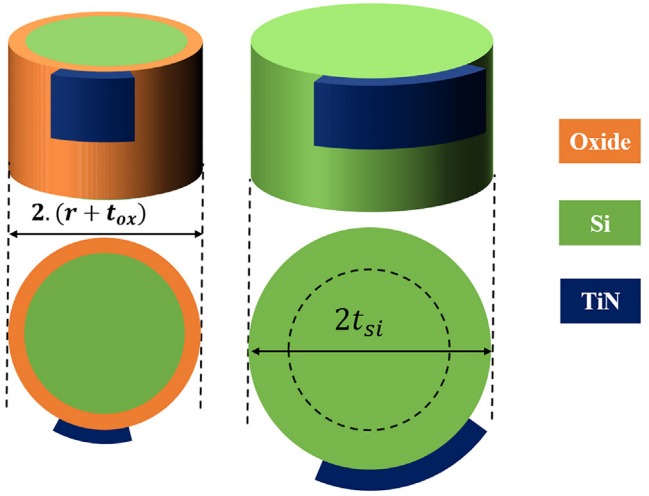

Fig. 2. Gate oxide on the Silicon nanowire is replaced by electrostatic equivalent thick silicon. The size of the grain is elongated by the factor η (only in azimuthal direction) due to this transformation.

Since the gate is wrapped around the nanowire, metal grains on the NWFET gate satisfies the periodic boundary condition in azimuthal (ϕ) direction for the Potential (V). The modified algorithm is presented below. The average grain diameter (S) is assumed to vary from 3 to 25 nm [11]. The 2D planar projection of the curved surface of the cylindrical gate is shown in Fig. 3(a).

1. The mean number of grains (N_G) on the gate of a single NWFET is determined using $N_G = \frac{4L_g \times (2\pi t_{si})}{\pi\eta S^2}$
2. The total gate area is discretized into a fine square mesh as shown in

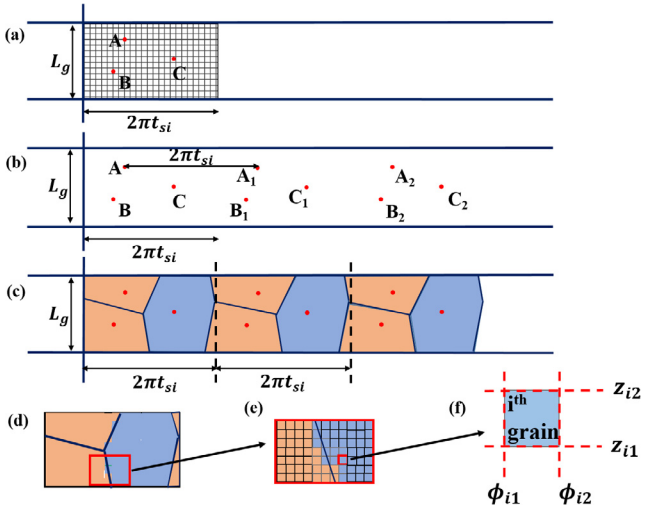

Fig. 3. Methodology to assign boundary conditions on Gate. (a) Gate area is discretized; and using Poisson distribution, integers are generated randomly and assigned to every grid point. Non-zero integer locations are highlighted with red dots. (b) For each grain center, a point is marked at a distance of $2\pi t_{si}$ and another at $2 \times 2\pi t_{si}$ and so on. (c) The blue solid lines represent perpendicular bisectors for the lines joining the dots. For each grain, WF is assigned based on probability. See the color assigned to each grain; (d) the marked section in figure (c) is selected as gate area. This selected area satisfies periodic boundary condition. (e) A representation of discretization a large Voronoi grain into tiny squares of appropriate WF; (f) The spatial coordinates (z_{i1}, z_{i2}, ϕ_{i1}, ϕ_{i2}) of ith grid point are shown. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)