

Invited Review

Digital and analog TFET circuits: Design and benchmark

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ABSTRACT

In this work, we investigate by means of simulations the performance of basic digital, analog, and mixed-signal circuits employing tunnel-FETs (TFETs). The analysis reviews and complements our previous papers on these topics. By considering the same devices for all the analysis, we are able to draw consistent conclusions for a wide variety of circuits. A virtual complementary TFET technology consisting of III-V heterojunction nanowires is considered. Technology Computer Aided Design (TCAD) models are calibrated against the results of advanced full-quantum simulation tools and then used to generate look-up-tables suited for circuit simulations. The virtual complementary TFET technology is benchmarked against predictive technology models (PTM) of complementary silicon FinFETs for the 10 nm node over a wide range of supply voltages (V_{DD}) in the sub-threshold voltage domain considering the same footprint between the vertical TFETs and the lateral FinFETs and the same static power. In spite of the asymmetry between *p*- and *n*-type transistors, the results show clear advantages of TFET technology over FinFET for V_{DD} lower than 0.4 V. Moreover, we highlight how differences in the I-V characteristics of FinFETs and TFETs suggest to adapt the circuit topologies used to implement basic digital and analog blocks with respect to the most common CMOS solutions.

1. Introduction

After the initial report in [1], complementary-metal-oxide-semiconductor (CMOS) transistors based on band-to-band-tunneling (BtBT), usually referred to as Tunnel-FETs (TFETs), have been extensively explored as possible replacements of, or complements to, conventional MOSFETs for low-power/low-energy electronic circuits targeting a supply voltage V_{DD} below 0.5 V [2–5]. TFETs embody a promising small slope FET concept able to achieve a subthreshold swing (SS) below the 60 mV/dec room temperature limit of conventional MOSFETs, as demonstrated by many theoretical works based on simulations (see [5] and references therein), and by some recent encouraging experimental results [6,7]. The lower SS compared to a conventional MOSFET can be exploited in two ways: if the threshold voltage is the same as in the MOSFET, the TFET will have a lower off-current (and thus lower static energy dissipation); if instead the same off-current is set in both devices, the TFET will be able to deliver a similar on-current as the MOSFET at a lower supply voltage V_{DD} , thus reducing both static and dynamic energy dissipations (which are proportional to V_{DD} and V_{DD}^2 , respectively). In this respect, circuit simulations have attributed to TFETs the potential to outperform conventional MOSFETs in the ultra-low voltage domain ($V_{DD} < 0.4$ V) in both analog [8–10] and digital

[11–17] applications. At higher supply voltages, however, the drive current of TFETs is significantly lower than the one of conventional MOSFETs. It is thus clear that TFETs can outperform MOSFETs only if they can deliver an SS significantly smaller than 60 mV/dec over a large current range in the subthreshold region. In many experiments this target has not been achieved, which may be due to fundamental as well as to material and device design issues [18–24]. As a result, the performance of the fabricated TFETs lags behind the optimistic figures reported in simulation studies, but experimental results have been steadily improving along the years. Another intrinsic advantage of TFETs over conventional MOSFETs stems from the lower temperature dependence of BtBT compared to thermionic emission [56], which may directly translate in less temperature sensitivity of TFET circuits. This has not been observed in early experimental reports about TFETs mainly because the conduction at very low current levels was often dominated by *Trap-Assisted-Tunneling* (TAT) and *Shockley-Read-Hall* (SRH) recombination processes [25]. Nevertheless, the fabrication process for TFETs is also getting more and more controlled and encouraging variability analysis are being reported both for statistically meaningful experimental samples [26], and for simulation based studies [27,28].

Among the possible technological platforms, silicon/silicon-

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germanium TFETs have the advantage of easy integration with mainstream CMOS [25,26,29,30]. However, the achieved performance is not very rewarding, especially for *n*-type TFETs, due to fundamental limit set by the indirect band-gap. As opposite to Si-based devices, TFETs based on heterojunction III-V structures are more promising [6,7,31,32] since they take advantage on their direct (and smaller) energy gap, and in fact they have shown higher on-current as well as SS below 60 mV/dec in the low current range. In addition, III-Vs provide more degrees of freedom for creating hetero-junctions and reduce ambipolar behavior.

The on-current and SS value are not the only important parameters to assess the possible advantages of TFETs against MOSFETs. TFETs are known to have a higher gate-drain capacitance [33], which can result in a switching time penalty compared to MOSFETs due to the Miller effect. On the other hand, the output conductance is lower due to the different electrostatics compared to MOSFETs [8]. Consequently, it is very important and timely to analyze the possible employment of TFETs in relevant benchmarking circuits. The fabrication processes for TFETs are however not as mature as for conventional CMOS transistors, and there exist very few reports about fabrication of TFET circuits (inverters in [25,34], current mirrors in [35], half-SRAM cell in [36]), in many cases employing transistors that are not at the state-of-the-art of TFETs and that are based on silicon platforms.

To assess the possible advantages of TFETs versus advanced CMOS transistors in realistic circuits, many simulation works have been presented. Most of such efforts have been devoted to digital circuits. SRAMs, for example, have been analyzed by various authors using different models for the TFETs either calibrated against experimental silicon devices [37] or obtained from full-quantum simulations [38]. Various SRAM topologies to circumvent the unidirectional conduction and/or to improve the cell stability have been also proposed [39–46]. Full-adders have been analyzed in [47–49] using look-up-tables (LUTs) obtained from TCAD simulations and calibrated against full-quantum results for hetero-junction complementary TFETs [50]. Level shifters have been also recently addressed in [50,51].

As for analog circuits, an operational transconductance amplifier (OTA) has been studied in [52], while a 6-bit successive approximation register (SAR) analog-to-digital-converter (ADC) has been simulated in [53] considering complementary double-gate GaSb-InAs hetero-junction TFETs. A thorough investigation in [54] analyzed mm-wave low noise amplifiers, oscillators, mixers, rectifiers and detectors using Verilog-A models for the hetero-junction GaSb-InAs TFETs presented in [55]. OTAs, current mirrors and track-and-old circuits based on InAs and GaSb/InAs TFETs have been analyzed in [8] using LUTs built from TCAD simulations calibrated on the device characteristics of [28,32]. Basic analog building blocks (current mirrors, differential pairs, diode-connected transistors) have been simulated in [56] using compact models calibrated on experimental strained silicon TFETs, proposing the deployment of TFETs in niche applications exploiting the lower temperature sensitivity. The performance of track and hold and comparators based on complementary heterojunction TFETs has been assessed in [9]. Different topologies of TFET-based power management circuits for energy harvesting applications have been proposed in [10,57]. Low-dropout linear voltage regulators with III-V TFETs have been analyzed in [58]. In most of these works, the characteristics of the *p*-TFETs are obtained by mirroring the ones of the *n*-TFETs.

In this paper, we present a comparison between aggressively scaled template heterojunction TFETs and FinFETs considering a wide variety of digital and analog/mixed-signal building blocks. The characteristics of the TFETs have been derived from full-quantum simulations [59], where *n*-TFETs and *p*-TFETs have been separately designed and have their own individual characteristics. This work reviews and extends previous publications from our group [9,37,47,48,51] by using the same set of devices for a large variety of circuits and supply voltages, and drawing more general conclusions. Furthermore, differently from the previous papers, the comparison with silicon FinFETs is carried-out at fixed occupied area and absolute off-current, hence essentially at the

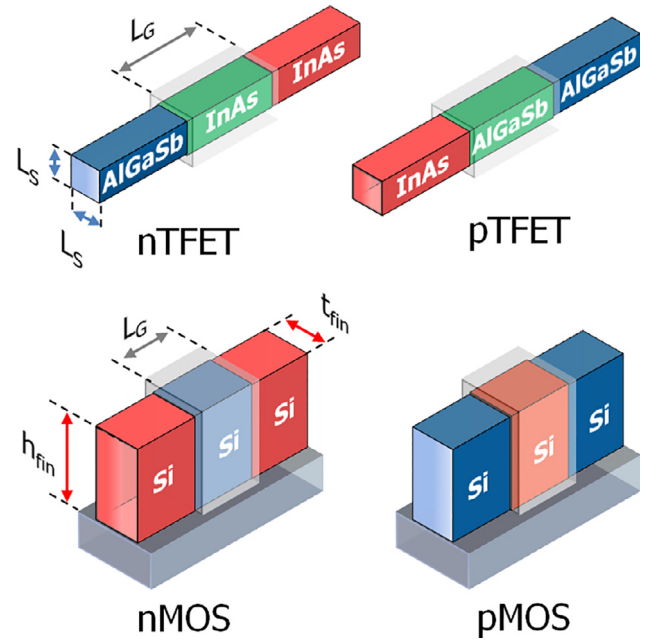


Fig. 1. Sketch of *n*- and *p*-type TFET and FinFET device architectures. The red and blue colors indicate the *n*- and *p*-doping types, respectively (green: intrinsic semiconductor, transparent-grey: oxide). TFET dimensions are: $L_G = 20$ nm, nanowire cross section (L_S) = 7 nm, EOT = 1 nm. FinFET dimensions are: $L_G = 14$ nm, $t_{fin} = 8$ nm, $h_{fin} = 21$ nm, EOT = 0.88 nm. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

same static power.

The paper proceeds as follows. The devices and the simulation methodology are described in Section 2. Simulation results for digital building blocks such as inverters, full-adders, SRAM cells and level shifters are reported in Section 3. Analog/mixed-signal building blocks (op-amps, current mirrors and comparators) are analyzed in Section 4. Conclusions are drawn in Section 5.

2. Virtual technology platforms and methodology for simulation and benchmarking

The geometric structures of the *p/n*-type nanowire (NW) TFETs and silicon FinFETs considered in the following of this work are shown in Fig. 1. The considered TFETs belong to the complementary virtual technology in [59], designed and characterized by means of full-quantum simulations. In particular, the AlGaSb/InAs NWs TFETs have a square cross section with a side $L_S = 7$ nm, a gate length $L_G = 20$ nm, and an equivalent oxide thickness EOT = 1 nm (with a physical oxide thickness of 2.3 nm by considering Al_2O_3 gate oxide [59]). The FinFET technology used as a benchmark was obtained via the PTM for 10 nm node FinFETs, available at [60]. There are two flavors of such a 10 nm node PTM-FinFETs targeting two different application domains: high-performance (HP) and low-standby-power (LSTP), the latter being the one selected for our analysis. FinFETs have fin height $h_{fin} = 21$ nm, fin width $t_{fin} = 8$ nm, $L_G = 14$ nm and EOT = 0.88 nm (physical oxide thickness of 1.2 nm [60]). As for the electrical characteristics, at the nominal V_{DD} of 750 mV, the *n*- and the *p*-FinFET feature a threshold voltage V_{th} of 425 mV and -428 mV, a saturation on-current I_{ON} of 44 μ A and -39.5 μ A, and an off-current I_{OFF} of 5.13 pA and -5.08 pA, respectively. Despite the different geometry, the benchmark is fair since the two architectures occupy almost the same area on the wafer under the assumption of having vertical TFET NWs (see for example [7]) and conventional lateral FinFETs. In fact, the physical footprint of a vertical TFET is a square with a total side of 11.6 nm (area ~ 135 nm²), considering the semiconductor wire and the surrounding Al_2O_3 gate oxide.

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