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Abstract

This work details the analysis of wafer level global process variability in 28 nm FD-SOI using split C-V measurements. The proposed approach initially evaluates the native on wafer process variability using efficient extraction methods on split C-V measurements. The on-wafer threshold voltage (V_T) variability is first studied and modeled using a simple analytical model. Then, a statistical model based on the Leti-UTSOI compact model is proposed to describe the total C-V variability in different bias conditions. This statistical model is finally used to study the contribution of each process parameter to the total C-V variability.

Keywords: Global variability, Split C-V, FD-SOI, Leti-UTSOI, modeling, characterization

1. Introduction

With decreasing critical dimensions of devices in advanced technology nodes, it is no longer possible to ignore the role of variability in ensuring reliability and performance of the designed circuits [1]. Evaluation of the impact of variability and development of mitigation methods are an important part of the development of sub 65 nm technology nodes [2]. The variability at circuit level can be broadly classified into global and local variability, depending on the scale at

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