Solid State Electronics 145 (2018) 54–57

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Performances of two-finger stacked fin quinary indium gallium zinc aluminum oxide thin-film transistors

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ARTICLE INFO

The review of this paper was arranged by Prof. E. Calleja

Keywords:
Induced channel layer
Quinary indium gallium zinc aluminum oxide materials
Stacked fin thin-film transistors

ABSTRACT

The two-finger stacked bottom gate and top gate fin indium gallium zinc aluminum oxide thin-film transistors (IGZAO TFTs) were fabricated. Since the bottom induced channel layer and the top induced channel layer were formed in the stacked TFTs using the bottom gate and the top gate, simultaneously. Consequently, drain-source current and transconductance of the stacked TFTs were enhanced about twice as those of the bottom gate TFTs and the top gate TFTs. The optimal performances of the stacked TFTs could be obtained, when the whole channel layer was induced as the carrier transportation path.

1. Introduction

In the past decades, thin-film transistors (TFTs) have been widely used in flexible electronics, radio frequency identification tags, smart cards, and display systems [1–3]. Among the channel material used in TFTs, the commonly used materials are amorphous silicon [4] and low temperature polycrystalline silicon [5]. However, the performances of the resulting TFTs suffered from the induced photocurrent generated by visible light due to their low bandgap energy. In view of the advantage of the high bandgap energy for preventing absorption of visible light, transparent metal oxide materials were developed and used as the channel film of TFTs, recently [6]. Due to high optical transmittance and reasonably high electron mobility, indium gallium zinc oxide (IGZO) materials were widely used in TFTs [7–9]. In the recent years, large frame size display systems and high pixel resolution display systems became prevalent. Therefore, high performance TFTs operated at a high operation current became a critical issue. The resulting IGZO TFTs still suffered from the long term stability problem caused by the oxygen vacancy in the IGZO channel films [10]. In view of the high binding energy of the Al-O bonds [11,12], quinary Al-doped IGZO (IGZAO) films were deposited to stabilize oxygen and improve stability [13]. High performance and stable IGZAO TFTs were also reported, recently [14,15]. In addition to, the dual gate TFTs were developed to improves the performance [16–18]. The top gate of the TFTs could assist to induce the channel layer and the top gate insulator could passivate the channel layer. Consequently, to enhance the operation current of stable IGZAO TFTs, the two-finger stacked bottom gate and top gate fin IGZAO TFTs were proposed and studied in this work.

2. Experimental details

Fig. 1 shows the schematic configuration of two-finger stacked bottom gate and top gate fin IGZAO TFTs. Bottom gate strips with a length of 25 µm and a width of 20 µm were patterned and formed on 150-nm-thick indium-tin-oxide (ITO) coated glass substrates using a standard photolithography method and a chemical etching solution of $HCl:HNO_3$:deionized water = 50:4:54, respectively. A 200-nm-thick HfO_2 film of bottom gate insulator and a 25-nm-thick Al film were then sequentially deposited by using a radio frequency (RF) magnetron cosputter. This cosputter was also used to deposit various-thick IGZAO channel layers on the HfO_2 bottom gate insulator. The IGZAO films were deposited using dual targets composed of IGZO (In:Ga:Zn = 3.52:1:2.72) target and Al target under an Ar/O_2 gas ratio of 60/40 and a working pressure of 100 mtorr. The RF power applied to the IGZO target and the Al target was 100 W and 50 W, respectively. The element atomic percent of In:Ga:Zn:Al:O = 20.45:5.57:15.47:1.31:57.20 in the deposited IGZAO films was obtained using the measurement of energy dispersive X-ray spectroscopy. The electron concentration and the electron mobility were 6.7×10^{16} cm^{-3} and 3.1 cm^2/Vs, respectively. The IGZAO channel region with a length of 25 µm and a width of 15 µm was patterned and formed on the front side of the central ITO gate using a standard photolithography method. Afterwards, a 75-nm-thick Al film was deposited using the RF magnetron cosputter. As shown in Fig. 1, the 75-nm-thick Al film was then patterned and formed into three 5-µm-wide Al strips using a standard

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https://doi.org/10.1016/j.sse.2018.04.008
Received 28 January 2018; Received in revised form 10 April 2018; Accepted 19 April 2018
Available online 23 April 2018
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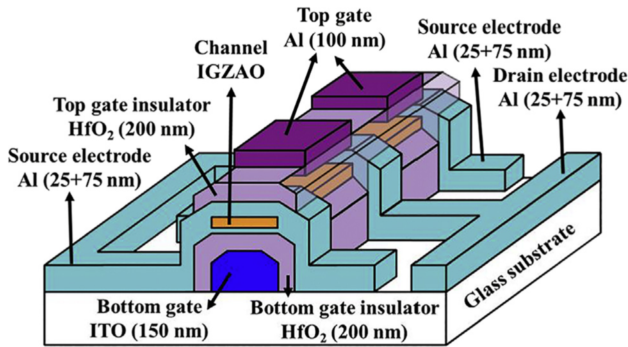

Fig. 1. Schematic configuration of two-finger stacked bottom gate and top gate fin IGZAO thin-film transistors.

photolithography method and a chemical etching process, respectively. It was worth noting that the fin IGZAO channel was surrounded by the whole Al metal shown Fig. 1. In the three Al strips, the central Al strip worked as the drain electrode and the other two Al strips worked as the source electrode of the bottom gate TFTs. The distance between the source electrode and the drain electrode was 5 μm. Moreover, a 200-nm-thick HfO_2 film of top gate insulator was deposited. Finally, a 100-nm-thick Al film of top gate metal was deposited and patterned on the front surface between the source electrode and the drain electrode of the TFTs. Consequently, the two-finger top gate TFTs were thus fabricated.

3. Results and discussion

The dependence of drain-source current (I_{DS}) on gate-source voltage (V_{GS}) of TFTs operated at a drain-source voltage (V_{DS}) in the triode region can be expressed as [19]:

$$I_{DS} = g_m\left[V_{GS}-\left(V_T + \frac{1}{2}V_{DS}\right)\right] \tag{1}$$

where g_m is transconductance and V_T is threshold voltage. To study the function of the thickness of IGZAO channel layer, 75, 60, and 25-nm-thick IGZAO channel layers were respectively deposited in the stacked TFTs. Furthermore, to verify the function of the stacked structure, the bottom gate TFTs, the top gate TFTs and the stacked TFTs were respectively biased and measured using an Agilent 4156C semiconductor parameter analyzer. Figs. 2, 3, and 4 show drain-source current-gate-source voltage ($I_{DS} - V_{GS}$) transfer characteristics of the IGZAO TFTs with 75, 60, and 25-nm-thick IGZAO channel layers operated at a drain-source voltage of 2 V, respectively. According to Eq. (1), by extrapolating the linear line in the $I_{DS} - V_{GS}$ transfer characteristics to the gate-source voltage axis as shown in Figs. 2, 3, and 4, the slope and the

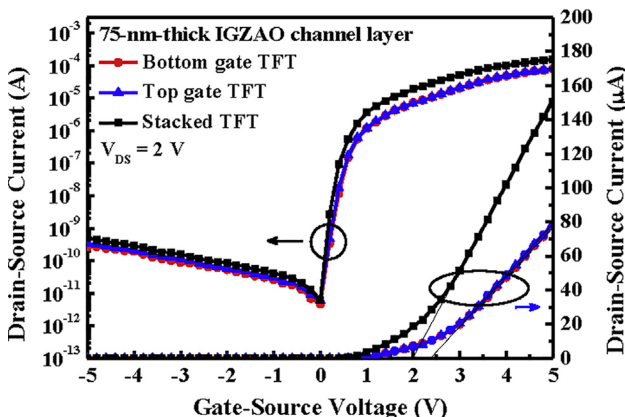

Fig. 2. Drain-source current-gate-source voltage transfer characteristics of IGZAO thin-film transistor with a 75-nm-thick IGZAO channel layer.

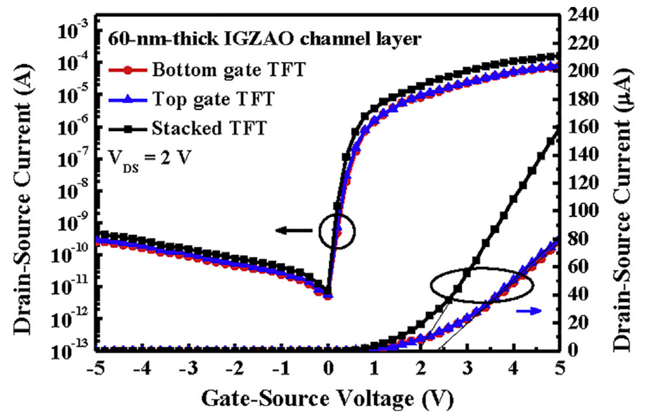

Fig. 3. Drain-source current-gate-source voltage transfer characteristics of IGZAO thin-film transistor with a 60-nm-thick IGZAO channel layer.

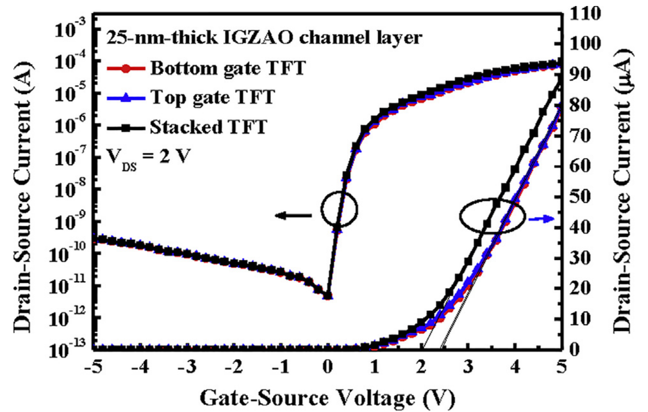

Fig. 4. Drain-source current-gate-source voltage transfer characteristics of IGZAO thin-film transistor with a 25-nm-thick IGZAO channel layer.

intercept value (X) were the transconductance g_m and the voltage of $V_T + V_{DS}/2$, respectively. If the TFTs operated at V_{DS}, the threshold voltage V_T could be obtained as $X - V_{DS}/2$. Furthermore, the subthreshold swing (S) was defined as $S = dV_{GS}/d(\log I_{DS})$. Table 1 listed the performances of the above-mentioned IGZAO TFTs. It was found that the threshold voltage of all the bottom gate and all the top gate TFTs with various channel layer thicknesses were at the same value 1.4 V. The subthreshold swing of the bottom gate and the top gate TFTs with 75, 60, and 25-nm-thick IGZAO channel layers were respectively kept at a similar value. The threshold voltage and the subthreshold swing of the stacked TFTs with 75 and 60-nm-thick IGZAO channel layers were improved to 1.0 V and 95 mV/decade, respectively. However, the threshold voltage was improved to 1.0 V and the subthreshold swing was kept at a similar value of 105 mV/decade for the stacked TFTs with 25-nm-thick IGZAO channel layer. For the bottom gate, the top gate, and the stacked TFTs with 75-nm-thick IGZAO channel layer biased at $V_{DS} = 2$ V and $V_{GS} = 5$ V, the I_{DS} was 78.3, 79.1, and 150.5 μA, and the g_m was 3.0×10^{-5}, 3.0×10^{-5}, and 4.9×10^{-5} S, respectively. For the corresponding three kind structured TFTs with channel layer thickness of 60 nm, the I_{DS} was 78.3, 80.0, and 158.2 μA, and the g_m was 2.9×10^{-5}, 3.0×10^{-5}, and 5.4×10^{-5} S, respectively. The I_{DS} and the g_m of the three kind structured TFTs with channel layer thickness of 25 nm were 79.0, 80.2, and 88.8 μA, and 2.9×10^{-5}, 3.0×10^{-5}, and 3.0×10^{-5} S, respectively. According to these measurement results, for the TFTs with the channel layer thickness of 75 and 60 nm, it was worth to note that the drain-source current of the stacked TFTs was about twice as that of the bottom gate TFTs and the top gate TFTs. The bottom gate TFTs and the top gate TFTs revealed the similar drain-source current under the same bias conditions. The on-

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