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Low-power logic computing realized in a single electric-double-layer MoS_2 transistor gated with polymer electrolyte

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ABSTRACT

Due to its mechanical flexibility, large bandgap and carrier mobility, atomically thin molybdenum disulphide (MoS_2) has attracted widespread attention. However, it still lacks a facile route to fabricate a low-power high-performance logic gates/circuits before it gets the real application. Herein, we reported a facile and environment-friendly method to establish the low-power logic function in a single MoS_2 field-effect transistor (FET) configuration gated with a polymer electrolyte. Such low-power and high-performance MoS_2 FET can be implemented by using water-soluble polyvinyl alcohol (PVA) polymer as proton-conducting electric-double-layer (EDL) dielectric layer. It exhibited an ultra-low voltage (1.5 V) and a good performance with a high current on/off ratio ($I_{on/off}$) of 1×10^5, a large electron mobility (μ) of 47.5 cm^2/V s, and a small subthreshold swing (S) of 0.26 V/dec, respectively. The inverter can be realized by using such a single MoS_2 EDL FET with a gain of ~4 at the operation voltage of only ~1 V. Most importantly, the neuronal AND logic computing can be also demonstrated by using such a double-lateral-gate single MoS_2 EDL transistor. These results show an effective step for future applications of 2D MoS_2 FETs for integrated electronic engineering and low-energy environment-friendly green electronics.

1. Introduction

Recently, two-dimensional (2D) transition metal dichalcogenides (TMDs) as a series of new materials have aroused widespread concerns due to their special electrical and optical properties [1–8]. TMDs possess a appropriate band gap of about 1–2 eV, showing potentially applicable in the field of nanoelectronics, photonics and sensing [9–15]. Specifically, TMDs-based FETs have been reported by different groups [16–23]. Among the different TMDs, one of the most promising materials is molybdenum disulphide (MoS_2) [9,24–29]. It has an indirect bandgap of 1.2 eV for bulk forms, and increase to 1.8 eV with a direct bandgap for the monolayer MoS_2 [28,29]. Up to now, MoS_2-based field-effect transistors (FETs) have attracted increasing attentions in many applications, for example, gas detectors [30], photo-electricity detectors [31] and logic circuit [32], etc.

Currently, electric-double-layer (EDL) transistors [33–36] has attracted many attentions relying on the use of gating media characterized by very high specific capacitance such as electrolyte materials and ion-gel dielectrics [37–44]. EDL transistors have considerable advantages. Firstly, electrolyte materials and ion-gel dielectrics have been widely investigated, as they exhibit very high specific capacitance values above 1 μF/cm^2 for films that can be thick and potentially printable using conventional methodologies [37–44]. It's reported that the high capacitance is due to the formation, upon polarization of the gel, of a very thin EDL (~1 nm) at the electrolyte-semiconductor interface following ion migration within the electrolyte and subsequent accumulation of carriers in the semiconductor [44]. Secondly, EDL transistors generally have lower operation voltage, which makes it possible for low-energy efficient electronic equipment. At the same time, logic circuit is a building block for integrated circuit including in the field of low-dimensional materials [45–47]. However, until now, few work was reported that polymer materials, including electrolyte materials and ion-gel dielectrics, have been used to realize logic functions in a single MoS_2 EDL transistor.

In this paper, logic functions in MoS_2 FET can be scaled down to a single transistor level by using water-soluble polyvinyl alcohol (PVA) as the proton-conducting EDL dielectric layer in MoS_2 FET. Such single MoS_2 FET exhibits a low operation voltage (~1.5 V) due to the formation of EDL after using PVA as a top dielectric layer. Based on this device structure, the inverter can be realized using such single MoS_2 FET with a gain of ~4 at the operation voltage of only ~1 V. Furthermore, the dynamic AND logic gate can be successfully implemented by a double-lateral-gate single MoS_2 EDL FET with such PVA protonic dielectric layer. These results show a vital step for future

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applications of 2D MoS_2-based FET for integrated electronic engineering, low-power sensors, and green flexible electronics.

2. Experimental details

Multilayer MoS_2 flakes were mechanically exfoliated by conventional Scotch-tape approach from bulk crystal and transferred subsequently to a slice of heavily doped silicon substrate with 300 nm SiO_2 capping layer. After proper MoS_2 flakes were selected under an optical microscope, 30-nm-thick Ni film was deposited by photolithography and thermal evaporation to prepare source/drain electrodes. 10 wt% PVA solution was then drop-casted onto the MoS_2 layer as the dielectric layer, which the powder of PVA was bought from Sigma-Aldrich company without any further process/purification. Atomic force microscopy (AFM) was used to measure the thickness of MoS_2 flakes, and the number of layers in MoS_2 was evaluated by Raman spectroscopy. The Hioki IM3539 LCR Meter is used to perform the frequency-dependent capacitance and phase angle measurements of PVA, and a Keithley 4200 semiconductor parameter analyzer is used to measure the I-V characteristics of the MoS_2 FET at room temperature in dark.

3. Results and discussion

The schematic diagram of traditional bottom-gated MoS_2 device structure can be found in Fig. 1(a), while the schematic diagram of top-gated MoS_2 transistor with PVA dielectric is shown in Fig. 1(b), respectively. In our device, two Ni electrodes were bridged by an exfoliated MoS_2 flake with a channel length of 6.65 μm and width of 4.78 μm, respectively. As shown in Fig. 1(c), the thickness of MoS_2 flake was estimated to be ~7 nm extracted by AFM image, which about 10 layers based on a 0.65 nm thickness per layer value [9]. The Raman spectroscopy of MoS_2 flake in our MoS_2 FET is shown in Fig. 1(d). The E^1_{2g} (384 cm^{-1}) and A_{1g} (409 cm^{-1}) modes are observed in the MoS_2 flake. Based on the previous report, the in-plane opposing motions of molybdenum and sulfur atoms is reflected by the vibration of $C_i = \frac{\varepsilon_0 \varepsilon_r}{d} = 1.15 \times 10^{-8}$ F/cm² mode, and that is the out-of-plane relative motions of sulfur atoms is reflected by A_{1g} mode [24,48]. The two sharp peaks of MoS_2 flake has almost the same peak distance ($\Delta_{peak\ shift} \approx 25\ cm^{-1}$) comparing the MoS_2 single crystal material, which indicate that MoS_2 flake has two typical characteristic peaks and thus negligible structural damages [49].

For examining the performance of the fresh MoS_2 device at room temperature, the output curves and transfer curve of MoS_2 FET are tested in the dark. Fig. 2(a) shows the output curves of traditional bottom-gated MoS_2 transistor measured by V_{DS} from 0 V to 5 V with a fixed V_{GS} from −10 V to 20 V, with 5 V steps. The corresponding transfer curve (log to linear) is shown by measuring the V_{GS} from −20 V to 20 V with a fixed V_{DS} bias of 0.1 V in Fig. 2(b). It clearly indicates that the MoS_2 device operated in a typical n-type enhancement-mode. Current on/off ratio ($I_{on/off}$) and subthreshold wing (S) are observed to be 3.6×10^4 and 5.42 V/dec, respectively. Than the threshold voltage (V_{th}) is extracted to be 16.21 V by extrapolating the linear portion of I_{DS}-V_{GS} curve to a zero drain current from the transfer curve. Finally, it can be accurately extracted the field-effect mobility (μ) base on the equation [50]:

$$\mu = \frac{L}{W \times C_i \times V_{DS}} \times \frac{dI_{DS}}{dV_G} \quad (1)$$

where the L is the MoS_2 channel length and W is the MoS_2 channel width, and $C_i = \frac{\varepsilon_0 \varepsilon_r}{d} = 1.15 \times 10^{-8}$ F/cm² is the SiO_2 dielectric capacitance ($\varepsilon_o = 8.85 \times 10^{-12}$ F/m represents the vacuum permittivity, $\varepsilon_r = 3.9$ represents the relative dielectric constant of SiO_2, and $d = 300$ nm represents the thickness of the gate insulator, respectively).

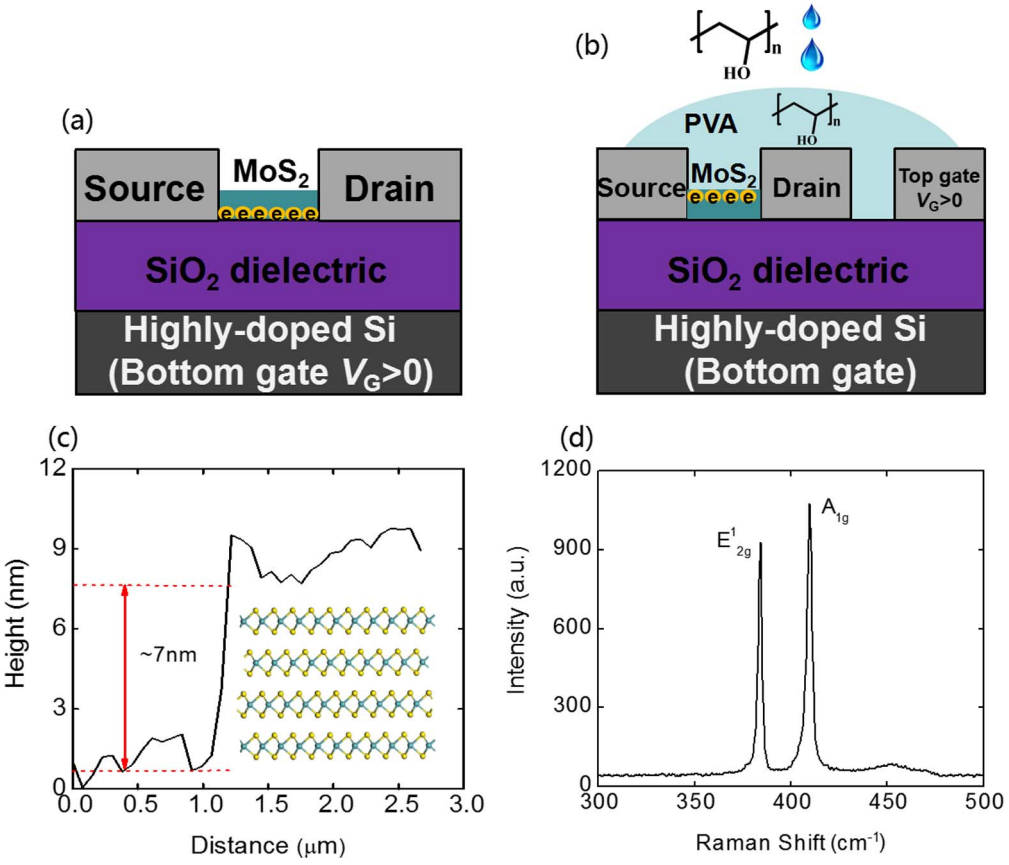

Fig. 1. (a) The schematic cross-section of multilayer MoS_2 transistor. (b) The schematic cross-section diagram of MoS_2 transistor using PVA as dielectric layer. (c) AFM image at the MoS_2 flake edge. (d) The Raman spectroscopy for the MoS_2 flake.