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Contacting graphene in a 200 mm wafer silicon technology environment

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ABSTRACT

Two different approaches for contacting graphene in a 200 mm wafer silicon technology environment were tested. The key is the opportunity to create a thin SiN passivation layer on top of the graphene protecting it from the damage by plasma processes. The first approach uses pure Ni contacts with a thickness of 200 nm. For the second attempt, Ni is used as the contact metal which substitutes the Ti compared to a standard contact hole filling process. Accordingly, the contact hole filling of this "stacked via" approach is Ni/TiN/W. We demonstrate that the second "stacked Via" is beneficial and shows contact resistances of a wafer scale process with values below 200 Ohm µm.

1. Introduction

Graphene has attracted a lot of attention for its unique physical properties [1,2]. The high electron mobility together with its two-dimensional structure makes it attractive for high speed electronic devices like graphene field effect transistors (GFET) [3,4]. Moreover the device concept of graphene base transistor as a vertical device was proposed to be even faster than GFETs using a very thin base of just one atomic layer of carbon for current modulation [5–7]. For all these device concepts reliable ohmic contacts to the graphene are desired. Recently good results were reached by applying different techniques [8–12].

Usually the integration of such devices in a baseline Si technology with several metal layers is required enabling for instance high frequency connections like thin film micro strip lines. Therefore an encapsulation of the graphene seems to be inevitable. Here we present a highly reliable passivation layer on top of the graphene to enable the processing in a CMOS production line with all the plasma based processes.

We discuss the experimental set-up with respect to the used equipment and present results of the electrical characterization of this wafer scale process.

2. Experimental set-up

Since the IHP is running a pilot line for the production of SiGe-BiCMOS [13] integrated circuits 200 mm Si-wafers were used as the industry-process compatible substrates for all the graphene processing. First a Ge-layer was epitaxial grown on the (1 0 0)-Si substrate wafers with low pressure epitaxy in Epsilon 3000 equipment from ASM. This layer has a thickness of 2000 nm to avoid the formation of SiC during the graphene epitaxy at high temperatures. The growth of the graphene layer was performed in an Aixtron Black Magic BM300 on these Ge (1 0 0) virtual substrates. Details about the growth process are published elsewhere [14]. The virtual substrate wafers with graphene on it were used as donor in a wet chemical transfer process. This transfer process [15] to insulating silicon dioxide substrate is necessary to proceed with the manufacturing of the devices. A poly(methyl methacrylate) (PMMA) based transfer process was used to handover the graphene to the target wafer with 100 nm thermal silicon oxide layer. Only the target wafer is used for further processing. At this stage the target wafer has already lithographic adjustment marks which make the alignment of other layers on top of the structured graphene possible.

2.1. SiN passivation as dielectric protection layer

An Applied Materials Silane DxZ chamber on a Centura mainframe was used for the depositions of silicon nitride on the patterned graphene. The plasma process was tuned to have a very low RF power [16]. This low RF power is necessary to avoid a damage of the graphene sheet [17] during the deposition of the silicon nitride dielectric. On the other hand the plasma-enhanced chemical vapor deposition (PECVD) process has the advantage of gas phase reactions which makes it independent from contact catalysis at the surface of graphene. Beside the fact that the SiN PECVD process is highly reproducible the variation of the layer thickness across the wafer shows a range of only 3 nm at

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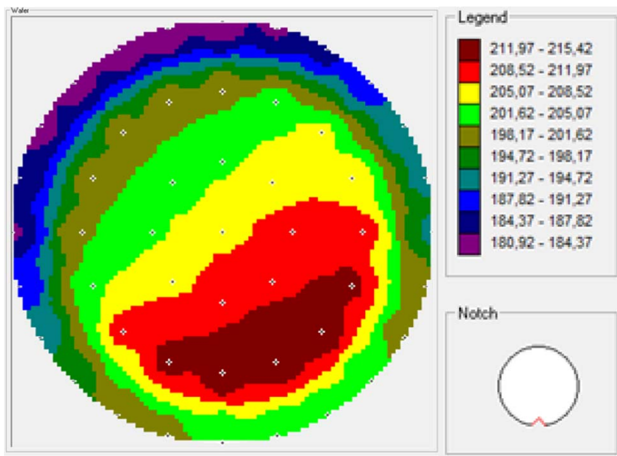

Fig. 1. Thickness map of silicon nitride film. The unit is Angstroms.

20 nm thickness target with radial symmetric distribution (see Fig. 1). The wafer-to-wafer non-uniformity is only 0.4%.

The graphene was characterized by Raman spectroscopy before and after the deposition of the dielectric layer. The results show no influence of the silicon nitride deposition on the graphene spectra (Fig. 2). Subsequently a SA-CVD (sub-atmospheric) chamber was used to deposit plasma-free SiO_2-layers by using Tetraethyl orthosilicate (TEOS) and ozone as precursors, but not directly on top of the graphene.

This additional silicon oxide deposition without plasma has no influence since the graphene layer is already protected by the silicon nitride layer which avoids the direct contact of graphene with oxygen radicals formed by the dissociation of ozone.

2.2. Contact process flow

Two different metallization schemes were used for the realization of TLM-structures to measure the contact resistance to graphene. The first approach is the direct contact of nickel lines to graphene. In this case two lithography mask steps are required (graphene and metal). The Ni is structured in a kind of damascene type process using CMP. For the second one a three mask process is used to realize graphene transmission line structures for electrical characterization of graphene. Here an additional via hole mask was applied.

A dry etch process with photo-resist mask is used to define graphene stripes for the TLM structures. The graphene stripes have a width of 2, 5, and 10 µm and a length of several hundreds of µm. More than 99% of the graphene is removed by this etch process. The remove of the resist requires special care because an ash process is forbidden by itself. We used wet clean techniques to remove all photo resist or PMMA residuals, respectively, from the graphene to ensure an intimate contact between the metal and the graphene later on.

After formation of the graphene stripes the silicon nitride is deposited to protect graphene against damages by the further processing. A 300 nm thick SA-CVD silicon oxide layer was deposited subsequently. The second lithography step is necessary to define contact holes to the graphene. The first step to open the contact holes is done by dry etching with an etch stop on the SiN to avoid the damage of the graphene by the harsh plasma. Wet etching with hot phosphoric acid was used for the final opening to graphene.

Due to the fact that the via hole is opened by an isotropic wet etch of silicon nitride one key parameter in this process flow is the wet etch rate of the SiN in phosphoric acid. The etch rate have been measured on test wafers after deposition of 100 nm of the low RF power SiN and a subsequent etch in phosphoric acid. The resulting wet etch rate on a 200 mm wafer is shown in Fig. 3. The proper adjustment of the etching time is important to have the contact vias open and immediately avoid large under etching beside the contact areas. The resulting under etch is shown in the cross section scanning electron microscopy image in Fig. 4. The under etch can be estimated to be 40 nm.

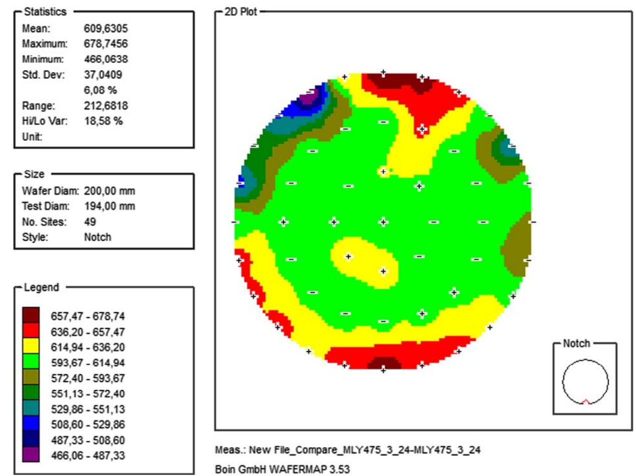

Fig. 3. Mapping of measured wet etch rates of low RF power SiN in hot phosphoric acid in Angstroms per minute.

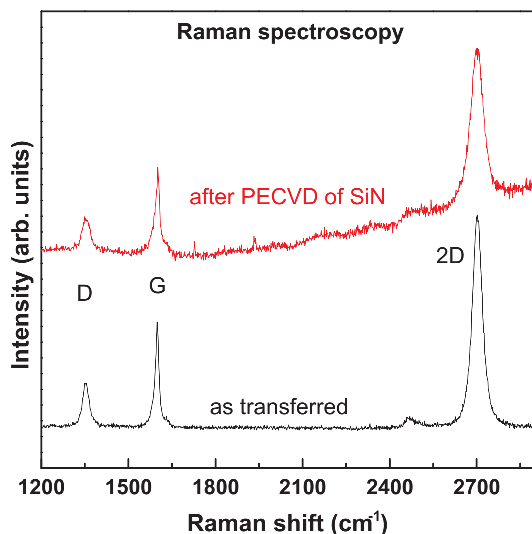

Fig. 2. Raman spectra of the graphene layers as transferred and after PECVD of SiN.

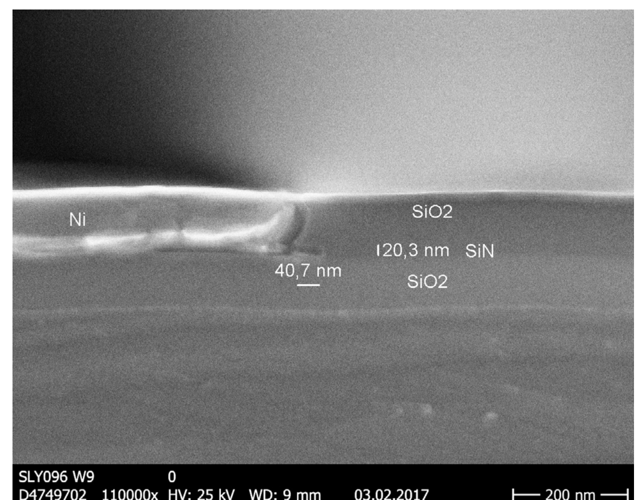

Fig. 4. Cross section scanning electron microscopy image showing the under etch into the SiN layer beneath the SiO_2 layer.

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