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Circular electrodes to reduce the current variation of OTFTs with the drop-casted semiconducting layer

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ABSTRACT

Circular organic thin film transistor (OTFT) structures are proposed to reduce the impact of variable grain alignment on the drive current of the polycrystalline organic thin film transistor (OTFT). As the circular structure is planar symmetric, the orientation of the grain cannot affect the drive current of the circular OTFT. Thus, circular electrodes expected to provide a lower variation. Top-gate, bottom-contact circular and conventional OTFTs with drop-casted polycrystalline 6,13-Bis(triisopropyl-silylethynyl) (TIPS)-Pentacene organic semiconducting layer (OSC) are fabricated to verify the theoretical variation reduction. The relative standard deviation (RSD), defined as the ratio of standard deviation and the average of drive current is used as the degree of variations in different structures. According to our fabrication result, circular transistors have a significantly lower variation (20% RSD), compared to the variation of conventional OTFTs (61% RSD).

1. Introduction

Variation is one of the major challenges for the future large-scale implementation of organic thin film transistor (OTFT) based circuits. Moreover, recent progress in the mobility of organic electronic materials made the variation bottleneck for the development OTFT based circuits [1–3]. Also, OTFTs are becoming popular as a future candidate for the low-cost printable circuits. Thus, printable solutions have more prospect towards the future development of organic transistor-based circuits.

Among the single crystal, polycrystalline and amorphous phases, the single crystal is not printable and amorphous have a very low mobility [4–6]. That is why the variation reduction of the polycrystalline organic semiconductors (OSC) based transistors are the best way for the consistent performance OTFT based circuits. Many solutions have proposed to decrease variation using a well-oriented polycrystalline grain [7–15]. However, all those solutions require additional and complex steps. Thus, the grain orientation is not controllable for the low-cost solution processed transistors.

Grain boundaries limit currents of the polycrystalline channel. A grain boundary contains a grain mismatch and irregularities at the inter-atomic distance. Grains of the printed OSC layers also exhibit a varying thickness of the semiconducting region. Whatever the irregularities are, the electrical representation of the grain boundaries is charge traps resulting the barrier. A carrier needs to pass different barriers for different grain orientations. Therefore, the flow of carrier remains unpredictable with the unpredictable grain orientation. D.T. James et al. [16] cast TIPS pentacene towards a certain direction. S. Wo [17] used a capillary tube for the deposition to align semiconducting layers. According to both investigations, the angle between writing direction and the C-C short axis is ± 28-degree. There exist twin boundaries between grain orientations of +28 and −28-degrees. Those twin boundaries can be avoided with proper alignments. Therefore, the total number of grain boundaries is lessened. J. Wade also found current maxima of TIPS pentacene OTFT for about 30-degree angle between grains and the OTFT channel-length [18].

Circular electrodes have been used in various electronic applications since 1990's. J.A. McAdoo et al. applied circular electrodes to lower capacitances, dark currents, and inductance of photodetectors [19]. K. Harada et al. proposed circular electrodes to increase air and water resistance of OTFTs [20]. Silicon-based concentric circular boundaries are designed to enhance the electrical reliability of the device by modulating the electric field at the drain end [23]. H. Lee et al. received enhanced drive current and stability with circular electrodes in silicon transistors [24]. E. Meijer et al. observed a lower parasitic leakage with the circular structure [25,26]. Therefore, we apply circular electrodes to reduce the grain-dependent current variation in addition to receiving other benefits of a larger source.

Our previous experiment with the coil-shaped electrodes, investigate that two transistors at 90-degree angle can reduce the

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orientation-dependent variation to one-fourth [27]. In that regard, the circular structure is much better as it can consider all angles. As a result, the angle-dependent variation becomes zero with circular structures. The circular electrode is resulting 20% relative standard deviation (RSD) on the drive current due to other variation sources.

2. Materials and fabrication sequence

To study the effect of grain arrangement and the advantage of proposed layout on OTFT characteristics, a generic process [27] is used to fabricate OTFTs on top of p-Si wafers covered by 1 μm SiO_2. The drop-cast method for the OSC deposition is selected instead of the spin-coat [28] for simplicity as well as to replicate the ink-jet printing process. 6,13-Bis(triisopropyl-silylethynyl) (TIPS)-Pentacene from Sigma-Aldrich, Cytop (poly-perfluoroalkenyl-vinylether) from Tokyo Chemical Industry and gold are used as the OSC layer, the dielectric and the electrodes respectively of the fabricated OTFTs [29]. The process is a top-gate bottom-electrode staggered combination with polymer dielectric to achieve better contacts [30,31] and smooth organic-dielectric interface. Oxygen plasma treatment using top-gate as the mask was used for etching the organic layer as well as the opening of the bottom electrode probing areas. Planned cross-sectional view of the conventional OTFT is shown in Fig. 1. Both conventional and circular OTFTs are fabricated on the same chip, following the same fabrication steps for a fair comparison. Metal lift-off for the top-gate after the Cytop dielectric deposition is the most unpredictable part of the fabrication. The Cytop layer is lifted with the acetone during the lift-off in roughly 27–21% chips. The probable reason for that phenomenon is the creation of pinhole in the Cytop layer. About 85% devices work properly at healthy chips.

Current-voltage characteristics are measured at room temperature in the ambient atmosphere and in the absence of light. The probe station with PSM-1000 microscope and the Agilent 4156C (precision semiconductor parameter analyzer) are used for measuring current–voltage characteristics. I_D-V_G curves are measured with 200 mV voltage-step and 20 ms time-step and voltages are swept from positive to negative.

3. Effect of grain boundaries on conventional transistors

A grain boundary contains a grain mismatch and irregularities at the inter-atomic distance. Charge trapping may occur at that irregularity. Grain boundary may also create a surface roughness, which causes a variable dielectric thickness over the channel [32–34]. All of these effects can be represented by the trapped charge, causes potential barriers for carriers while passing the channel. That trapped-charge representation does not indicate the presence of trapped charges. Each of the abovementioned physical situations can create a barrier against the flow of carriers. That barrier is similar to the barrier caused by trapped charges. Potential barriers are increasing the threshold voltage and decreasing the mobility. Due to the variation in the size of grains, heights of barriers, the orientation of barriers and the number of barriers polycrystalline transistors are facing a significant percentage of variation.

Grains of a drop-casted OSC are parallel to each other over a small area and for a single OTFT that orientation is constant over the entire channel region in most of the cases. The inset of Fig. 2 presents fabricated OTFT with a constant grain orientation over the channel. Fig. 2 presents transfer characteristics of 60 conventional transistors. ON current of transistors is the current at $V_G = -40$ V, and $V_D = -25$ V. The relative standard deviation among measured 60 transistors is 61%.

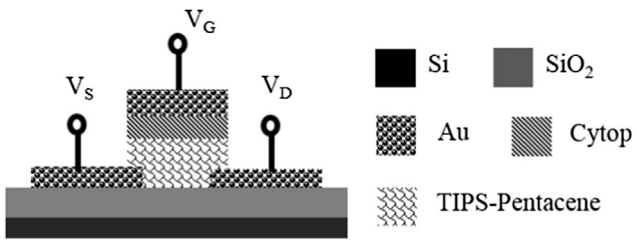

Fig. 1. Cross-sectional view of OTFT (not to scale).

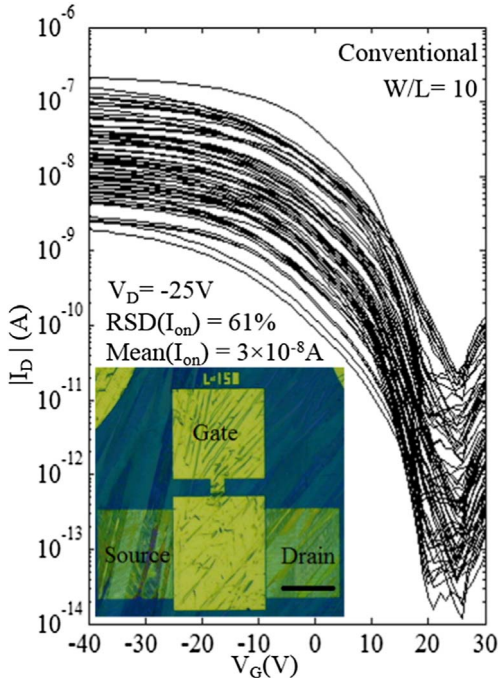

Fig. 2. The transfer characteristics of 60 conventional OTFTs. Inset presents optical photo fabricated OTFT. L = 150 at the top of optical image indicates that the channel length is 150 μm. The scale-bar at the bottom-right corner of inset represents 100 μm.

4. Average mobility of multiple transistors at different angles

In our previous study [27] we prove that variation is reduced by two transistors at a 90° angle. The calculation of two transistors at 90° is much easier because if one transistor is maintaining θ angle with the grain, another transistor is maintaining 90°- θ angle with the grain. When considering three or more transistors uniformly placed at different angles, we need to assign angles considering 360°. While using three transistors, angles between two consecutive transistors become 360°/3 = 120°. While using five transistors, angles become 360°/5 = 72°. Fig. 3 presents the sketch of multiple transistors at different angles. Table 1 presents the effect of multiple transistors at different angles. Transistors numbers are varied from 1 to 9 except 4, 6 and 7 transistors. With uniformly placed three transistors the RSD value is decreased from 59.2% to 5.92%. The effect of four transistors at 360°/4 = 90° angles is equal to two transistors at the 90° angle. Thus, four transistors at ninety-degree give the same theoretical variation compared to two transistors at ninety-degree. Similarly, 6 transistors give the same variation of three transistors and, thus not mentioned at the table. As 360°/7 is not an integer and cannot be expressed with a few digits, it is difficult to find adjustable points and that point is not mentioned. With 9 electrodes, the theoretical variation becomes less than 1%.

As a circular transistor can be represented as a large group of transistors, uniformly distributed along different angles and it can make the theoretical angle-dependent variation to zero. Moreover, as the structure is a top gate type and the semiconducting area is irregular, the dielectric layer is also of irregular thickness and that thickness variation is lower along grains. Therefore, that thickness dependent variation is also reduced with circular electrodes. However, there are other sources

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