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New Insights on SOI Tunnel FETs with Low-Temperature Process Flow for CoolCube™ Integration

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Abstract

This paper reports the fabrication and electrical characterization of planar SOI Tunnel FETs (TFETs) made using a Low-Temperature (LT) process designed for 3D sequential integration. These proof-of-concept TFETs feature junctions obtained by Solid Phase Epitaxy Regrowth (SPER). Their electrical behavior is analyzed and compared to reference samples (regular process using High-Temperature junction formation, HT). Dual I_D-V_{DS} measurements verify that the TFET structures present Band-to-Band tunnelling (BTBT) carrier injection and not Schottky Barrier tunnelling. P-mode operating LT TFETs deliver an ON state current similar to that of the HT reference, opening the door towards optimized devices operating with very low threshold voltage V_{TH} and low supply voltage V_{DD}.

Keywords: Tunnel FET, TFET, SOI, low temperature, SPER, tunnelling, BTBT, CoolCube™, 3D sequential integration

I. INTRODUCTION

Tunnel FETs (TFETs) are reverse-biased gated p-i-n diodes (Fig. 1) yielding extremely low OFF currents and, in theory, low subthreshold swing (SS) below the CMOS 2.3·kT/q limit [1]–[7]. These properties render TFETs very attractive for ultra-low power applications (V_{DD} < 0.4 V). TFETs exhibit significant differences with respect to regular CMOS devices: i) The ON state current is generated by band-to-band tunnelling (BTBT) carrier injection and ii) a single TFET device can be used either in p- or n-operation mode. TFETs can been fabricated on Si or SOI platforms with regular CMOS process flow (*i.e.*, using high temperature steps for gate stack, spacers, epitaxy and junctions) [4], [6], [8], [9]. Other materials, device architectures and processing steps have been proposed to enhance performance [10]–[15]. Nevertheless, the compatibility with CMOS is a key asset, and compatibility with novel low-temperature 3D integration techniques is also a plus.

Low-temperature processes have been demonstrated to be suitable for 3D sequential integration (CoolCube™) [16]. In a recent work [17], we have presented preliminary results on Tunnel FETs fabricated with a low temperature (LT) process. This paper aims at providing additional analysis and details, focusing on the compatibility of LT TFETs with 3D sequential integration. These LT devices are also compared to regular high temperature (HT) TFETs. Besides electrical measurements, TCAD simulations have been carried out to reveal the junction-related electrical differences between HT and LT devices.

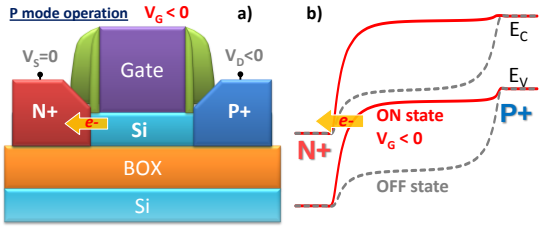

Fig. 1. *a)* TFET bias scheme for p-mode operation; *b)* Corresponding band diagram illustrating the OFF state (dashed grey lines: the distance between the N^+ and P^+ regions is too long for BTBT to occur) and ON state (solid red line: abrupt P^+-N^+ junction achieved by expanding the P^+ region under the gate due to formation of a hole inversion layer for V_G < 0).