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The prospects of transition metal dichalcogenides for ultimately scaled CMOS

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ABSTRACT

MOSFET gate length scaling has been a main source of progress in digital electronics for decades. Today, researchers still spend considerable efforts on reducing the gate length and on developing ultimately scaled MOSFETs, thereby exploring both new device architectures and alternative channel materials beyond Silicon such as two-dimensional TMDs (transition metal dichalcogenides). On the other hand, the envisaged scaling scenario for the next 15 years has undergone a significant change recently. While the 2013 ITRS edition required a continuation of aggressive gate length scaling for at least another 15 years, the 2015 edition of the ITRS suggests a deceleration and eventually a levelling off of gate length scaling and puts more emphasis on alternative options such as pitch scaling to keep Moore's Law alive. In the present paper, future CMOS scaling is discussed in the light of emerging two-dimensional MOSFET channel, in particular two-dimensional TMDs. To this end, the scaling scenarios of the 2013 and 2015 ITRS editions are considered and the scaling potential of TMD MOSFETs is investigated by means of quantum–mechanical device simulations. It is shown that for ultimately scaled MOSFETs as required in the 2013 ITRS, the heavy carrier effective masses of the Mo- and W-based TMDs are beneficial for the suppression of direct source-drain tunneling, while to meet the significantly relaxed scaling targets of the 2016 ITRS heavy-effective-mass channels are not needed.

1. Introduction

Over decades, MOSFET scaling has been the major driver in digital electronics and for a long time scaling was tantamount to gate length scaling. As shown in Fig. 1, the gate length in commercial integrated logic circuits has been reduced from about 5 µm in 1975 down to sub-30 nm in 2010. This translates into an exponential reduction of the gate length, accompanied by an exponential growth of the number of transistors integrated on a single Si chip, a trend colloquially called Moore's Law. Also shown in Fig. 1 are the scaling targets of the ITRS (International Technology Roadmap for Semiconductors) [1], the evolution of the gate length for scaled laboratory stage MOSFETs, and predicted scaling limits.

Scaling has never been an end in itself. Instead, the main motivation for scaling was and still is of economic nature. As pointed out by Gordon Moore already in his classical paper from 1965 [2], enhancing the complexity of integrated circuits, i.e., increasing the number of transistors per chip, by proper scaling leads to an exponential decrease of the cost per transistor. Thus, scaling scenarios are always influenced by economic consideration in addition to aspects of technology improvements and device physics.

During the past few years, the future of gate length scaling is seen less optimistically than in the past [7,8] and contradictory trends can be observed. On the other hand, the envisaged scaling scenario for the next 15 years has undergone a significant change. While the 2013 ITRS edition still required an aggressive continuation of gate length scaling for at least another 15 years (i.e., until the year 2028), the 2015 edition of the ITRS expects a deceleration and eventually a levelling off of gate length scaling at around 10 nm in 2020. Moreover, alternative options to keep Moore's Law alive such as pitch scaling and three-dimensional integration gain popularity [9,10]. On the other hand, at the laboratory stage device engineers have achieved remarkable progress in further gate length scaling, well-performing ultra-scaled MOSFETs with sub-5 nm gate lengths [4,5] have been reported, and novel channel materials for MOSFETs are explored. Here, particularly the 2D (two-dimensional) materials have attracted a lot of attention [11]. The most recent achievement in gate length scaling was the demonstration of a 1-nm gate MOSFET with 2D MoS_2 channel [6].

The present paper provides a condensed overview of 2D materials and, given the fact that today the TMDs (transition metal

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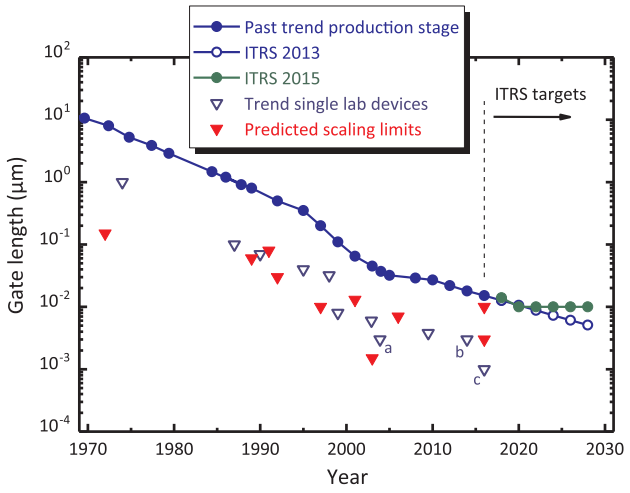

Fig. 1. Evolution of gate length scaling. After [3], updated. (a) 3-nm gate Si MOSFET (NEC, 2003 [4]). (b) 3-nm gate V-groove SOI MOSFET (AIST, 2014 [5]). (c) 1-nm gate MoS_2 MOSFET (UC Berkeley, 2016 [6]).

dichalcogenide) represent the most prominent class of 2D materials, of the state of the art of TMD MOSFETs. Furthermore, future CMOS scaling is discussed in the light of the emerging TMDs considering both the ITRS 2013 and ITRS 2015 scaling scenarios.

2. Overview of 2D materials and 2D transistors

For decades, Si has been dominating the semiconductor world unchallenged. In 2004, however, the pioneering work on the preparation of graphene [12,13], a material consisting of a single layer of carbon atoms arranged in a hexagonal 2D lattice, brought a new class of materials, namely the 2D materials, into the focus of semiconductor research. Graphene shows exceptional electronic properties like an ultrahigh carrier mobility leading to early expectations that it could be the perfect channel material for future MOSFET generations and possibly replace the conventional semiconductors in electronics. Due to its zero gap, however, which impedes proper switch-off of MOSFETs for digital logic and deteriorates the performance of radio frequency MOSFETs, graphene could not fulfill the high expectations [14]. Just when the interest of the transistor community in graphene began to subside, the demonstration of single-layer MoS_2 FETs [15] gave new momentum to the research on 2D materials. Over a short period of time, entire classes of new 2D materials have been discovered and meanwhile hundreds of 2D materials are under investigation. Moreover, many groups worldwide explore the potential of the 2D materials for electronic devices, in particular MOSFETs. Fig. 2 shows important classes of 2D materials, together with representative materials for each group, and gives an impression on the lively research activities in the field.

Table 1
Gate length, thickness and material of the gate dielectric, gate configuration (BG – backgate, TG – top-gate), channel thickness, subthreshold swing, and drain-induced barrier lowering of scaled planar MoS_2 MOSFETs.

L (nm)	Gate oxide	Gate configuration	t_{ch} (nm)	*SS* (mV/dec)	*DIBL* (mV/V)	Ref.
10	5 nm HfO_2	TG	4–5	250	50	[17]
10	7.5 nm HfO_2	BG	4–6	200	240	[20]
10	5–6 nm Al_2O_3	TG	0.65	250	–	[21]
10	6 nm Al_2O_3	TG	0.65	180	–	[22]
8.6	6 nm HfO_2	TG	0.65	140	290	[23]
7.5	10 nm HfO_2	BG	2	120	700	[24]
1	5.8 nm ZrO_2	BG	1.3	65	290	[6]

When analyzing the literature it appears that currently TMD MOSFETs, in particular those with Mo- and W-based TMD channels (with MoS_2 MOSFETs being the frontrunners), attract most attention. Since the demonstration of the first TMD MOSFET, a 500-nm gate monolayer MoS_2 transistor in 2011 [15], a continuously increasing number of groups has successfully been fabricating TMD MOSFETs and MoS_2 MOSFET scaling down to below 10 nm gate length has been pursued intensively. Table 1 shows information on recently reported MoS_2 MOSFETs. Particularly impressing is the 1-nm gate MoS_2 MOSFET from [6] showing astonishingly good switch-off, an excellent minimum subthreshold swing *SS* of 65 mV/dec, and an average *SS* of 115 mV/dec over five decades of drain current variation. Its drain-induced barrier lowering *DIBL* of 290 mV/V, on the other hand, is rather modest. Regarding *DIBL*, the 10-nm gate MoS_2 MOSFET from [17] showing a *DIBL* of only 50 mV/V is worth mentioning. This transistor, however, suffers from a rather large *SS* of 250 mV/dec. For comparison, a 3.8-nm gate length Si tri-gate MOSFET showing an *SS* of 92 mV/dec and a *DIBL* of 150 mV/V [18] and a 20-nm gate Si nanowire gate all around MOSFET with *SS* = 60 mV/dec and *DIBL* = 52 mV/V [19] have been reported recently. It should be noted that these Si MOSFETs possess multi-gate architectures while all MoS_2 MOSFETs from Tab. I are single-gate devices. Moreover, the data from Tab. I does not show a clear correlation between gate length, gate oxide thickness, and number of MoS_2 layers stacked one on top of the other in the channel (which equals t_{ch}/0.65 nm, where t_{ch} is the channel thickness and 0.65 nm is the thickness of a MoS_2 monolayer). This means that obviously there is still much room for optimizing the device structures and improving the performance of MoS_2 MOSFETs. It should be stressed, on the other hand, that

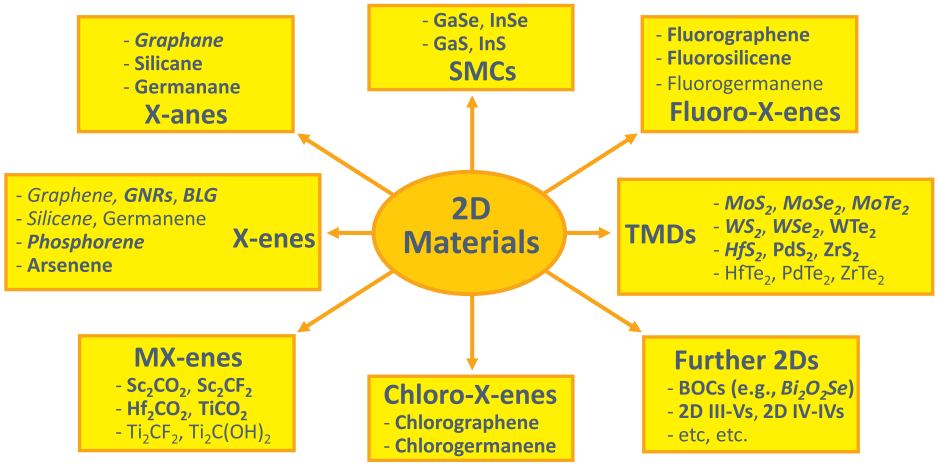

Fig. 2. Classes and representative examples of 2D materials. SMC: Semimetal chalcogenide. GNR: Graphene nanoribbon. BLG: Bilayer graphene. BOC: Bismuth oxychalcogenide. Bold: 2D materials with sizable bandgap. Italic: 2D materials already used in experimental MOSFETs. After [16], updated.