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Indium-oxide nanoparticles for RRAM devices compatible with CMOS back-end-off-line

Edgar A.A. León Pérez[a,*], Pierre-Vincent Guenery[a], Oumaïma Abouzaid[a], Khaled Ayadi[a], Solène Brottet[a], Jérémy Moeyaert[b], Sébastien Labau[b], Thierry Baron[b], Nicholas Blanchard[c], Nicolas Baboux[a], Liviu Militaru[a], Abdelkader Souifi[a]

[a] Univ. Lyon, Institut des Nanotechnologies de Lyon-UMR CNRS 5270, INSA Lyon, 69621 Villeurbanne, France
[b] Univ. Grenoble Alpes, CNRS, CEA/LETI Minatec, LTM, F-38054 Grenoble Cedex, France
[c] Univ. Lyon, Institut Lumière Matière-UMR CNRS 5306, UCBL1, 69621 Villeurbanne, France

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ABSTRACT

We report on the fabrication and characterization of Resistive Random Access Memory (RRAM) devices based on nanoparticles in MIM structures. Our approach is based on the use of indium oxide (In_2O_3) nanoparticles embedded in a dielectric matrix using CMOS-full-compatible fabrication processes in view of back-end-off-line integration for non-volatile memory (NVM) applications. A bipolar switching behavior has been observed using current-voltage measurements (I-V) for all devices. Very high I_{ON}/I_{OFF} ratios have been obtained up to 10^8. Our results provide insights for further integration of In_2O_3 nanoparticles-based devices for NVM applications.

1. Introduction

Among new emergent memory technologies, such as Magnetic RAM (MRAM) or Conductive Bridge RAM (CBRAM), Resistive Random Access Memory (RRAM) technology appears as a suitable candidate for the next generations of non-volatile memories (NVM) due to the commutation between two resistive states when thin layers of metal oxides are used in metal-insulator-metal (MIM) structures (two terminal devices) [1–5]. Furthermore, it has been reported that the integration of nanoparticles in these devices might allow the reduction of the tunnel oxide thickness without compromising data retention, which directly accounts for the scalability and performance of such devices [6–14].

In this work, that is an extended and completed version of the results presented in [15], we show In_2O_3 nanoparticle (NPs)-based RRAM devices for CMOS back-end-off-line integration in future NVM technology. In_2O_3 is a suitable material due to its electron affinity (3.3–4.45 eV) and work function (~5 eV) [16–19]. These parameters directly account for the conduction-band-offset with the tunnel and control oxides, and so for the charge retention on memory capacitor-like structures.

We propose an insulating-NPs-insulating system which benefits from the above-mentioned characteristics for data retention. The fabricated RRAM devices ($Au/Cr/Al_2O_3/In_2O_3$-NPs/SiO_2/Si-n+, see Fig. 1(a)) exhibited bipolar switching behavior for different device-sizes (circular-shaped electrodes), going from D = 500 µm down to D = 30 µm.

2. Experiments

The above-mentioned-two-terminal-device architecture was fabricated using n+-type silicon substrates (0 0 1). The first step of the process is the thermal oxidation of the substrate, leading to the formation of a 2-nm-thick layer of high quality SiO_2 (tunnel oxide). Indium nano-sized droplets are directly grown on the oxide surface at low-temperature (< 450 °C) by metal-organic-chemical-vapor-deposition using a 300 mm-MOCVD reactor from Applied Materials. The system is then cooled down to room temperature and exposed to ambient atmosphere, leading to the formation of In_2O_3 NPs on the SiO_2 surface. Fig. 1(b) shows an atomic force microscope (AFM) scan of these NPs with heights comprised between 9 nm and 14 nm, and an estimated density of 3×10^8 NPs/cm^2. Subsequently, an Al_2O_3 layer (control oxide) is deposited by atomic layer deposition (ALD) at 200 °C with an Ultratech/CNT Fiji series reactor, using trimethylaluminum and H_2O reactors in thermal mode. Two different Al_2O_3 layers were used: 1.5 nm and 6 nm, corresponding to 25 and 100 cycles of ALD-process.

For electrical characterizations, 200 nm-thick gold circular top electrodes were deposited with an Edwards thermal evaporator using a shadow mask. The electrodes nominal-diameters were comprised

* Corresponding author.
E-mail address: edgar.leon-perez@insa-lyon.fr (E.A.A. León Pérez).

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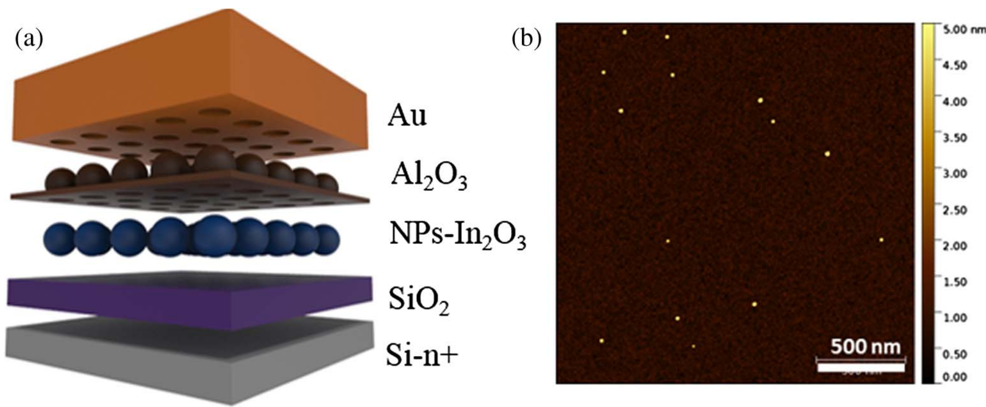


Fig. 1. (a) Schematic structure of the fabricated devices, and (b) AFM cartography of one device after In_2O_3 NPs formation on top of SiO_2 surface.

between 500 µm and 30 µm. Finally, a rapid thermal annealing stage (RTA, ADDAX) of 10 min at 400 °C, under N_2 atmosphere, was used to passivate the electrical contacts. Once the devices were finished, silver paste was used to fix the devices to a sample holder, in order to facilitate its manipulation and to have an ohmic contact with the n + -Si substrate.

Current-voltage measurements were then recorded using a Keithley 4200 semi-conductor parameter analyzer at room temperature (300 K). Measurements were done with a power-gradual increase frame, i.e. for an applied bias sweep range and a fixed current compliance (I_c), if no resistive switch-behavior appeared, then the amplitude of the applied bias was first increased. If still no resistive switch-behavior was observed, and instead current values reached I_c, then the value of I_c was progressively increased. The process was repeated until a resistive switch-behavior appeared, or until the device was definitely damaged. Capacitance-voltage measurements were also recorded using an Agilent 4284A system.

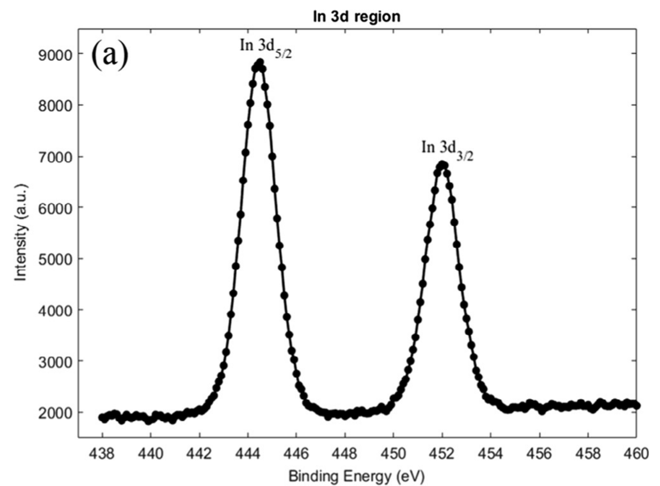
X-ray photoelectron spectroscopy (XPS) and cross-section observations by transmission electron microscopy (X-TEM) were performed in order to study the presence of In-O bindings in the In_2O_3 NPs and to visualize their morphology, respectively.

3. Results and discussions

3.1. Morphological characterizations

Prior to full-device fabrication XPS analysis and TEM observations were effectuated. First, XPS analysis were performed after the NPs synthesis on a 2 nm-thick SiO_2 layer in order to investigate the chemical composition of the NPs. Fig. 2(a) shows the survey spectrum in the In 3d region. The binding energies of In $3d_{5/2}$ and In $3d_{3/2}$ were found at 444.5 eV and 452.1 eV of the photoemission spectrum, respectively, showing good agreement with the literature ([20] and references therein). This information confirms the presence of the In-O bonding in the NPs.

Second, for TEM observations, three control samples were fabricated with NPs directly synthesized on a 100 nm-thick SiO_2 layer: (i) “as is”, i.e., In_2O_3 NPs are found on the surface of the SiO_2 layer, (ii) an Al_2O_3-1.5 nm-thick ALD layer is deposited on the NPs (Fig. 2(b) shows a cross-sectional image of this sample where several NPs are observed), and (iii) the same Al_2O_3 deposition is made plus an RTA stage used for the devices-fabrication (400 °C for 10 min). Fig. 2(c)–(e) show a cross-sectional TEM image of these samples, respectively. In_2O_3-NPs are hemispherical, and the surface of the Al_2O_3 control oxide is conformal. In Fig. 2(e) white broken lines were added in order to identify the Al_2O_3 layer. Amorphous and crystalline phases were observed for the NPs. In Fig. 2(c)–(e) it can be clearly distinguished that the NP are in a crystalline phase and the lattice fringe periodicity can be attributed to the (2 2 2) cubic In_2O_3 plane, which is one of the most intense diffraction



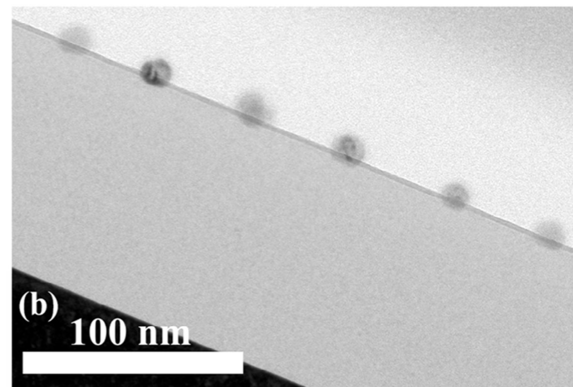


Fig. 2. (a) XPS analysis of nanoparticles: XPS survey in the indium 3d region where two binding energies where observed at 444.5 eV and 452.1 eV, confirming the presence of the In-O bonding. X-TEM images of different samples where In_2O_3 NPs are synthesized on a 100 nm-thick SiO_2 layer: (c) “as is”; (b) and (d) correspond to a sample where an Al_2O_3 ALD layer was deposited on the NPs; and (e) the same Al_2O_3 deposition is made and the sample undergoes also an RTA annealing at 400 °C for 10 min (closest configuration to final devices).

direction for this oxide [21,22]. It is worth mentioning that we have observed, not systematically, that under the influence of electron beam, amorphous In_2O_3 nanoparticles crystalize. Furthermore, it has been observed for the three samples that an interaction between the SiO_2 and the NPs can take place, since it is observed that a part of the NP is found in the SiO_2 layer, as it can be seen in Fig. 2(d) and (e). This might be explained by the fact that indium is a highly reactive element, which can induce oxygen pumping from the SiO_2 layer, leading to the diminution of the thickness of the latter and to the formation of In_2O_3 in it. Therefore, special attention must be paid for the devices with a low

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