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Kink effect in ultrathin FDSOI MOSFETs

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ABSTRACT

Systematic experiments demonstrate the presence of the kink effect even in FDSOI MOSFETs. The back-gate bias controls the kink effect via the formation of a back accumulation channel. The kink is more or less pronounced according to the film thickness and channel length. However, in ultrathin (< 10 nm) and/or very short transistors (L < 50 nm), the kink is totally absent as a consequence of super-coupling effect. For the first time, thanks to the availability of body contacts, the body potential is probed to evidence the impact of majority carrier accumulation and drain pulse duration on the kink effect onset.

1. Introduction

The kink effect is a well-known floating-body mechanism in partially-depleted (PD) SOI MOSFETs: majority carriers, generated by impact ionization and stored within the body, increase the body potential and lower the threshold voltage [1–5]. More carriers are available for impact ionization and further increase the body potential. This feedback mechanism results in a sudden increase in drain current that is beneficial for current drive and speed in logic circuits. It is however detrimental for the linearity of analog circuits.

The kink effect has also been observed in relatively thick fully depleted (FD) SOI MOSFETs, where the back gate was used to convert FD operation into PD mode [6]. A negative back-gate voltage enabled the storage of enough holes near the back Si-BOX interface such as to trigger the kink [6,7]. It is widely believed that ultrathin FDSOI transistors are kink-free. This myth is inaccurate being contradicted by other floating-body effects which have been demonstrated in FD-SOI (GIFBE [8] or linear kink [9], MSD [10], parasitic bipolar [11], etc.)

In this work, we revisit the kink effect and bring novel information from several angles:

– The experimental conditions enabling the activation of the kink effect in state-of-the-arts FDSOI N-channel MOSFETs with thickness from 25 nm to 8 nm are investigated (Section 3).
– The body potential is monitored and correlated with the drain current variation.
– Pulse measurements are performed in order to control the amount of majority carriers generated by impact ionization and stored in the body (Section 4).
– Experiments and TCAD simulations (Section 5) indicate the variation of the kink voltage with back bias, pulse duration, channel length and film thickness.
– The absence of kink in transistors thinner than 10 nm is explained by the onset of the super-coupling effect.

2. Experimental details

Several generations of FDSOI MOSFETs have been examined. The thickness of Si film t_{Si} varied from 25 nm down to 8 nm and the buried oxide (BOX) was 25 nm thick. The fully depleted film was either unintentionally doped (background doping of $N_A \sim 10^{15}\ cm^{-3}$) or lightly doped ($N_A \sim 10^{17}\ cm^{-3}$). The FDSOI process at STMicroelectronics included high-k/metal gate stack with thin or thick dielectric. We probed n-channel devices with variable gate length down to $L_G = 40$ nm. Back-gate bias V_{Gb}, ranging from 0 V to −10 V was applied through a highly doped ground plane ($N_A \sim 10^{18}\ cm^{-3}$). Five terminal body-contacted devices were also probed for direct measurement of the body potential.

3. DC measurements

3.1. Floating-body transistors

Fig. 1 shows typical output $I_D(V_D)$ characteristics of 25 nm thick transistor. In normal operation with grounded back-gate ($V_{Gb} = 0$), there is no kink effect. On the other hand, for negative back-gate bias, a

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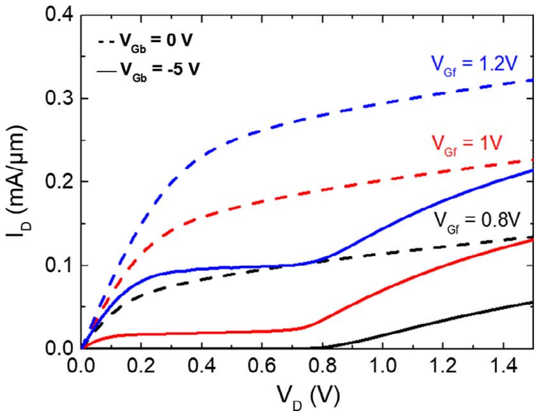

Fig. 1. Output $I_D(V_D)$ characteristics with back-gate voltage $V_{Gb} = 0$ and $V_{Gb} = -5$ V. W = 10 µm, L = 100 nm, t_{si} = 25 nm, t_{ox} = 2.9 nm, 25 nm BOX thickness.

marked kink effect develops for $V_D \sim 0.7$–1 V (Fig. 1). The amplitude and onset of the kink depend on front-gate bias (Fig. 1) and back-gate bias as shown in Fig. 2.

The kink is accentuated by the interface coupling effect: a negative back bias increases the front-channel threshold voltage and lowers the drain current. Fig. 2a and b shows that for $V_{Gb} < -5$ V, the drain current seems to jump from 'zero' (sub-threshold value) to a high value (strong inversion). In short transistors (L_G = 50 nm, Fig. 2c), the kink is clearly attenuated.

Fig. 3 shows in detail the role of channel length. In very short-channel MOSFETs (L = 40–50 nm), the kink is hardly detectable for several reasons:

(i) The potential barrier at the source is lower than in long transistors. This drain-induced barrier lowering (DIBL) enables the holes generated by impact ionization to escape through the forward-biased source junction instead of accumulating in the body.

(ii) The large output conductance induced by DIBL can mask the kink-related current increase; the competition between kink and DIBL is visible in Fig. 2c.

(iii) The accumulation of holes is weakened by the proximity of the source and drain junctions. The lateral fringing fields, from source/drain through the substrate and BOX, modify the body potential [12,13] and attenuate the impact of back-gate bias in short-channel devices [14]. It follows that the influence of back-gate on kink is attenuated.

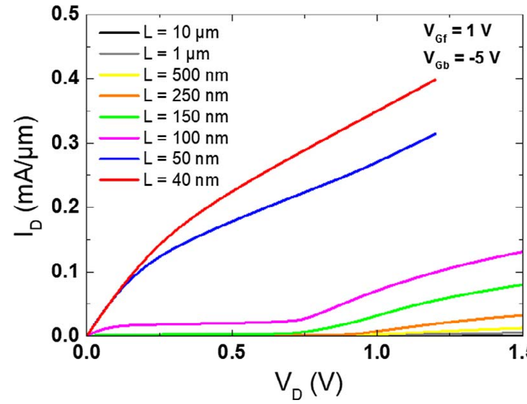

Fig. 3. $I_D(V_D)$ curves showing the kink effect dependence on channel length. W = 10 µm.

The critical voltage V_C for kink onset is defined as the inflection point in $I_D(V_D)$ curves (see Fig. 4(a)), in other words the position of the conductance-peak. At constant gate voltage, V_C decreases slightly in shorter devices (Fig. 4b) where the lateral field and impact ionization are stronger, shifting the kink onset to lower drain bias.

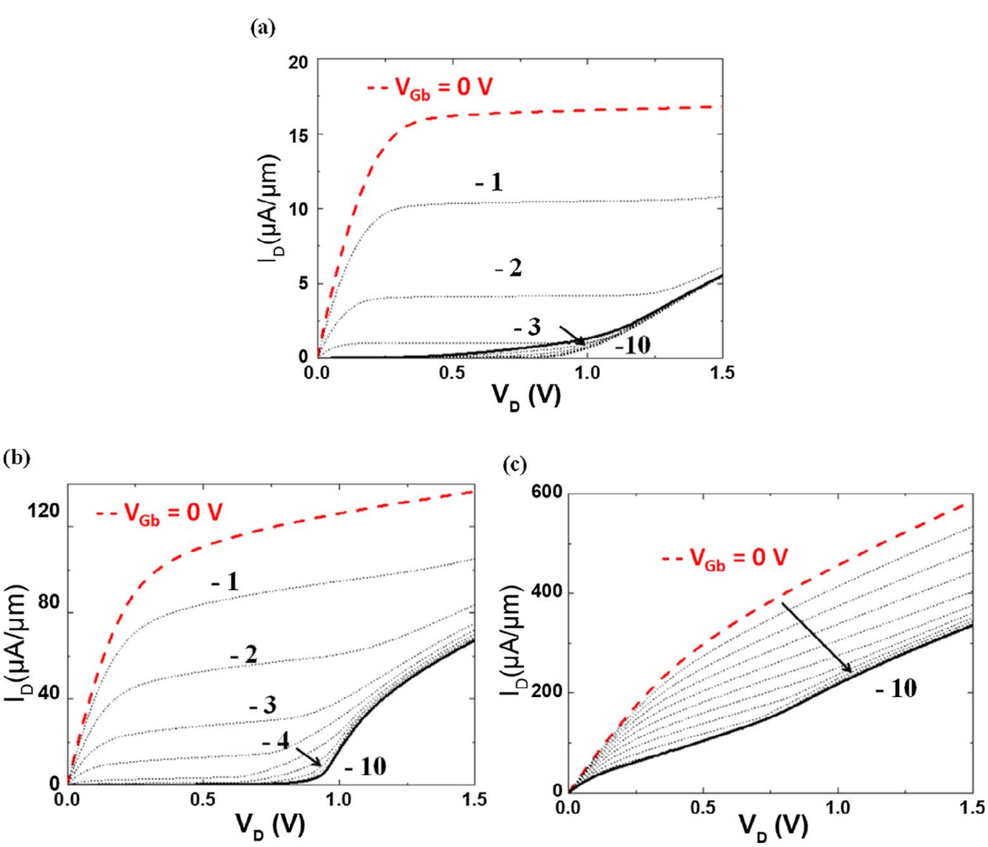

Fig. 2. Impact of back-gate bias V_{Gb} from 0 V to −10 V (step −1 V) on $I_D(V_D)$ characteristics for various channel lengths: (a) 1 µm, (b) 150 nm, and (c) 50 nm; t_{si} = 25 nm. V_{Gf} = 1 V.