Solid State Electronics xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Insight into carrier lifetime impact on band-modulation devices

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ARTICLE INFO

Keywords:
Z^2-FET
SOI
Band modulation
Hysteresis
Carrier lifetime
Generation-recombination
Diffusion

ABSTRACT

A systematic study to model and characterize the band-modulation Z^2-FET device is developed bringing light to the relevance of the carrier lifetime influence. This work provides guidelines to optimize the Z^2-FETs for sharp switching, ESD protection, and 1T-DRAM applications. Lower carrier lifetime in the Z^2-FET helps in attaining the sharp switch. We provide new insights into the correlation between generation/recombination, diffusion, electrostatic barriers and carrier lifetime.

1. Introduction

Ultra-Thin Body and Buried oxide (UTBB) devices emerged as promising candidates for the next-generation low-power applications thanks to their attractive features: resilience against short-channel effects and parasitic capacitances, performance improvement by back biasing, threshold voltage tuning, economical (planar) manufacturing process, higher mobility and near-ideal switching characteristics [1]. The versatility and flexibility of the UTBB have made possible the fabrication of innovative devices such as band-modulation Z^2-FET (Zero Impact Ionization and Zero Subthreshold Slope Field Effect Transistor). Z^2-FET, a partially gated PIN diode, is one amongst the family of sharp-switching devices that has shown promising applications in electrostatic discharge (ESD) protection circuit and 1T-DRAM (Single - Transistor Dynamic Random Access Memory) especially for low-power internet of things (IoT) applications [1–8]. Z^2-FETs are shown to maintain their excellent switching characteristics in advanced technological nodes (14 nm and 28 nm FDSOI) [8]. Z^2-FET works by modifying the forward bias operation of PIN diode and fashioning electrostatic barriers with the help of front-gate (V_{GF}) and back-gate (V_{GB}) voltages. The current blocking is achieved by creating a thyristor (n-p-n-p) like structure via gate controlled band-modulation. The flattening of these induced electrostatic barriers results in a sharp switch of the current level of the diode.

Previous works on Z^2-FET focused upon introducing the concept of band-modulation and positive feedback that primarily govern the Z^2-FET operation [2], showcasing the device as one of the local strategic solutions for ESD protection circuits [4] and its capability to be used as 1 T-DRAM [5,6]. Z^2-FET was shown to maintain reliable operation for a wide range of temperatures (86–398 K) [7]. Technological advancement from 28 nm to 14 nm aided into the device performance [8] and encouraged the authors to further explore the possibility of variation in the device design to add more functionality [8,9]. Recently, a very detailed analytical model was proposed that covers all operational regimes of Z^2-FET [10]. In this work we have explored the key reason behind the exceptional performance of Z^2-FET and pointed out how it is being benefitted by the advancement of technology.

The blocking and unblocking of the current in Z^2-FET is a complexed physical phenomenon that is governed by the balance and imbalance between generation-recombination (G-R) and diffusion currents in the DC operation, and by non-equilibrium mechanisms in pulsed mode [10]. Carrier lifetime plays an essential role in governing these processes. For instance, the blocking of the carriers is favorable only when their diffusion length (controlled by carrier lifetime) is within the order of channel length. Carrier lifetime is said to be degraded in thinner films (advanced technological nodes) due to the

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https://doi.org/10.1016/j.sse.2017.12.007

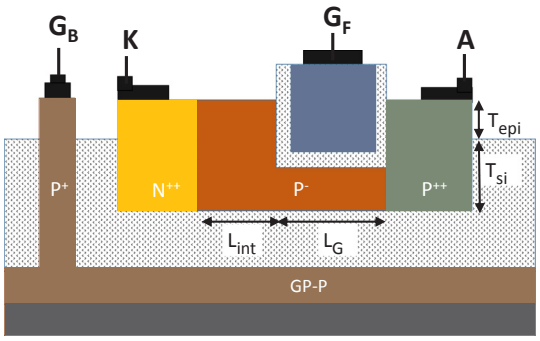

Fig. 1. Schematic diagram of the measured/simulated device.

contribution of surface recombination. In ultrathin SOI films, the lifetime is actually dominated by the interface G-R velocity. The article highlights how the degradation of the lifetime is beneficial for this innovative Z^2-FET architecture and explores its effect on the operation of sharp-switching devices.

The paper is organized as follows. Section 2 depicts the device structure and the experimental characterization. In Section 3, a detailed study (characterization and working principles) of Z^2-FET is presented with the help of TCAD simulations. On purpose, we have introduced carrier lifetime as a central parameter and, showed how device characteristics in DC and transient mode can be modulated. Section 4 elaborates on the role of lifetime in device operation.

2. Device description and characterization

The schematic of measured/simulated Z^2-FET is shown in Fig. 1. These devices are fabricated in the 28 nm FDSOI technology node with ultrathin silicon film (T_{si} = 7 nm) and thin buried oxide (T_{BOX} = 25 nm). Raised epitaxial layer (T_{epi} = 15 nm) in the anode, cathode, and ungated regions reduces the series resistance. The top of the channel is partially covered with a gate composed of metal and high-k dielectric with an EOT of 1.4 nm. The lengths of the gated region (L_g) and ungated region (L_{int}) are 200 nm. The underlying p-type ground plane with a doping of 10^{18} cm^{-3} works as back-gate for the device.

Fig. 2 shows hysteresis in experimental anode current (I_A) − anode voltage (V_A) characteristics for various front-gate voltages. The back gate bias V_{GB} is kept at −1 V for all experiments and simulations. For increasing V_A, unlike standard PIN diode, Z^2-FET remains off until the turn-on voltage (V_{on}) is reached. At V_{on}, the current undergoes a sharp transition turning the device on. V_{on} strongly depends upon the applied gate voltages. A typical value of V_{on} is higher (by 0.1–1 V) than the silicon diode turn-on voltage, depending upon the applied V_{GF}. The

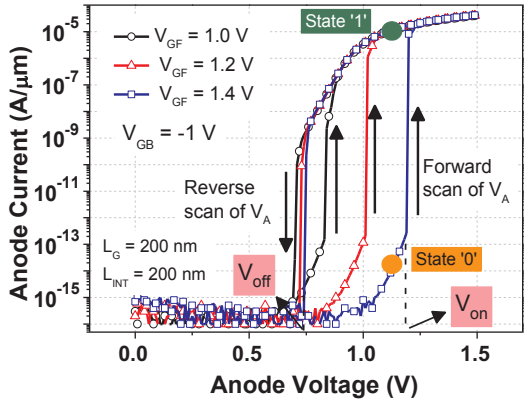

Fig. 2. Experimental hysteresis in I_A-V_A curves of Z^2-FET for different V_{GF}.

occurrence of the steep switch also differentiates Z^2-FET from standard diode operation. The reverse sweep, i.e. the decrease in anode voltage, results in different turn off voltage (V_{off} < V_{on}) exhibiting hysteresis. The width of the hysteresis window increases with V_{GF} as a result of the progressive shift of turn-on voltage (V_{on}) due to stronger barriers created by gates. The hysteresis facilitates two different current states ('1' and '0') corresponding to high or low current levels for the same value of anode voltage, making Z^2-FET as an attractive choice to design low power 1T-DRAMs [2].

3. Simulation and device operation

To understand the details of the Z^2-FET operation and particularly the role of the lifetime, 2D simulations are performed with Synopsys TCAD simulator [11] using standard models of doping and mobility (doping dependence, Philips unified mobility, high-field velocity saturation, and transverse field dependence). To capture the effect of carrier generation-recombination in the silicon-based Z^2-FET, doping and temperature dependent Shockley–Read–Hall (SRH) recombination model is included. The doping dependence of SRH lifetime is modeled with Scharfetter relation [11] given by,

$$\tau_{dop(N_A+N_D)} = \tau_{min} + \frac{\tau_{max}-\tau_{min}}{1+\left(\frac{N_A+N_D}{N_{ref}}\right)^{\gamma}} \quad (1)$$

where the default value of τ_{max} is 10^{-5} s and τ_{min} is 0 s. As this work addresses the impact of lifetime, a range of values from 10^{-6} s to 10^{-10} s are selected for τ_{max} for electrons. For holes, τ_{max} is taken as 0.3 times of the τ_{max} for electrons (default value). τ_{min} is kept at 10^{-12} s. The default value of gamma (γ = 1) is used in the simulations. Interface charge density (Q_{ox}) is from 10^{11} to 2×10^{12} cm^{-2}. Both Q_{ox} and τ_{max} are considered as the tuning parameters for the calibration of simulation data. Density gradient model is also utilized to include the effect of quantum confinement of the carriers especially in the channel region with a thickness of 7 nm.

Diffusion length of the carriers, which plays an essential role in device operation, depends upon mobility and lifetime. To distinguish the effect of both parameters, in Section 3.3, different (fixed) values of mobility are considered keeping the lifetime constant.

3.1. DC characteristics

To simulate the DC I-V curves for Z^2-FET two approaches were followed: (1) Voltage ramping and, (2) Current ramping. The characteristics for voltage ramp failed to converge at the steep transition point. To avoid convergence failure in the voltage ramp, a slow anode voltage transient is applied. Prior to this slow V_A ramp (50 s from 0 V to 2 V), fast transient (10 ns) pulses were applied at both gates (V_{GF}, V_{GB}) to emulate the realistic biasing approach of measurements (Fig. 3a). The obtained hysteresis (Fig. 3b) between the increasing and decreasing ramp of anode voltage is similar to the experimental data (Fig. 2). On the other hand, the characteristics achieved by ramping up the anode current were S-shape snapback curves (Fig. 3b). It is interesting to note that the snapback, which depicts the negative resistance region, is embedded within the hysteresis window. Voltage ramping method fails to trace this S-shape curves as several values of current correspond to a single voltage value in the snapback region, and from the best of our knowledge, this problem cannot be supported by this TCAD tool yet. Nevertheless, the hysteresis and snapback reveal same phenomena within the device achieved by two different characterization techniques. Fig. 3b is plotted for the two different values of carrier lifetime (τ_{max} = 10^{-10} s and 10^{-9} s). Qualitatively, I-V characteristics are similar for both values of τ_{max}. The reason for different values of V_{on} and the holding current (constant current before V_{on}, see Fig. 7) is explained in Section 4 in detail.

The important point to be noted here is that the inversion charge