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Static and low frequency noise characterization of ultra-thin body InAs MOSFETs

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ABSTRACT

A complete static and low frequency noise characterization of ultra-thin body InAs MOSFETs is presented. Characterization techniques, such as the well-known Y-function method established for Si MOSFETs, are applied in order to extract the electrical parameters and study the behavior of these research grade devices. Additionally, the Lambert-W function parameter extraction methodology valid from weak to strong inversion is also used in order to verify its applicability in these experimental level devices. Moreover, a low-frequency noise characterization of the UTB InAs MOSFETs is presented, revealing carrier trapping/detrapping in slow oxide traps and remote Coulomb scattering as origin of 1/f noise, which allowed for the extraction of the oxide trap areal density. Finally, Lorentzian-like noise is also observed in the sub-micron area devices and attributed to both Random Telegraph Noise from oxide individual traps and g-r noise from the semiconductor interface.

1. Introduction

The necessity of pursuing Moore's Law while surpassing the limitations of Silicon, led to the study of new materials and processes for metal oxide semiconductor transistors. For example, III–V materials like InAs and InGaAs are widely regarded as leading candidates for increased drive current digital applications [1–3]. Indeed, effective mobility values over 3000 $cm^2/V\,s$ i.e. much higher than in silicon MOSFETs at a comparable sheet density, and, volume oxide trap densities around $10^{19}/eV/cm^3$ have been reported in [2,3]. The accurate determination of the electrical parameters in such novel devices is essential for understanding their physical properties. In this context, the goal of the paper is to apply characterization techniques that are already established for Si MOSFETs in order to study the behavior of ultra thin body InAs MOSFETs.

2. Devices and experimental details

The devices measured in this work are ultra thin body (UTB) InAs MOSFET transistors with MBE selectively raised InAs n+ Source/Drain (S/D) contacts on lattice mismatched InP/InAs/InGaAs/InAlAs/InP epilayer [4]. The high k gate stack is composed of Al_2O_3 (2 nm) and HfO_2 (2 nm). The capacitance equivalent thickness of the structure (CET) is around 1.7 nm. The channel length L varies from 1 μm down to 0.025 μm while the channel width W is fixed at 3 μm. Drain current measurements in the linear (V_d = 30 mV) and saturation regions (V_d = 1 V) were performed with Agilent B1500 Semiconductor Device Analyzer, whereas the drain current noise was measured using the Agilent B1530 Waveform Generator Unit.

3. Results and discussion

3.1. Parameter extraction

Typical I_d–V_g characteristics at V_d = 30 mV are presented in Fig. 1 both in linear and logarithmic scale for different gate lengths. In order to extract the device parameters, we applied the Y-Function method (Eq. (1)) in strong inversion for several gate lengths (see Fig. 2) [5].

$$Y = \frac{I_d}{\sqrt{g_m}} \tag{1}$$

In a previous work, it has been shown that the Lambert-W (LW) function can describe very well the inversion charge Q_i from weak to strong inversion [6]:

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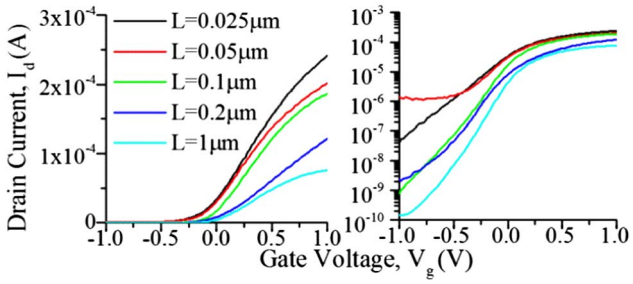

Fig. 1. Experimental transfer characteristics for UTB InAs n-MOSFETS.

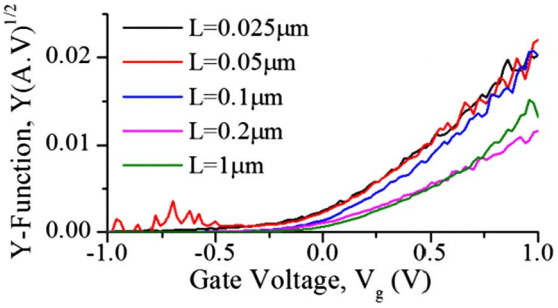

Fig. 2. Y-V_g characteristics for UTB InAs n-MOSFETS.

$$Q_i(V_g) = C_{ox}\cdot\frac{\eta kT}{q}\cdot LW\left(e^{\frac{q\cdot(V_g-V_t)}{\eta kT}}\right) \tag{2}$$

where C_{ox} is the gate oxide capacitance per unit area, kT the thermal energy, η the subthreshold ideality factor and V_t the threshold voltage.

The drain current of a MOSFET in linear operation is given by Eq. (3):

$$I_d = \frac{W}{L}\mu_{eff} Q_i V_d \tag{3}$$

where V_d is the drain voltage. The effective mobility, μ_{eff}, can be expressed with the inversion charge:

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1\frac{Q_i}{C_{ox}}+\theta_2\left(\frac{Q_i}{C_{ox}}\right)^2} \tag{4}$$

where μ_0, is the low field mobility, θ_1 and θ_2 are the first and second order mobility attenuation factors, respectively. Indeed, we applied the methodology described in [6] to verify the applicability of this method in these experimental level devices. Impressively, as shown in Fig. 3, using the best fit parameters we managed to have a very good agreement between the experimental and the modeled $I_d(V_g)$ curves from weak to strong inversion.

As can be seen in Fig. 4, the threshold voltage V_t and low-field mobility μ_0 values extracted from LW lie close enough to those obtained from Y-function, yet being reasonably unequal, concerning the

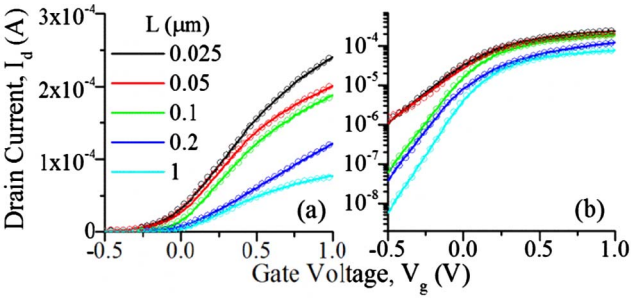

Fig. 3. Experimental (symbols) and LW-fitted (lines) transfer characteristics for UTB InAs n-MOSFETS.

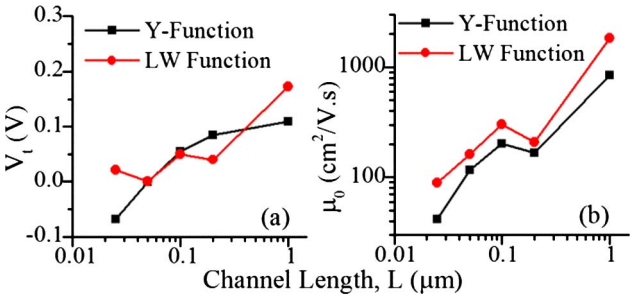

Fig. 4. Variation of V_t (a) and μ_0 (b) extracted from Y-Function (black lines) and LW-Function (red lines) with L. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

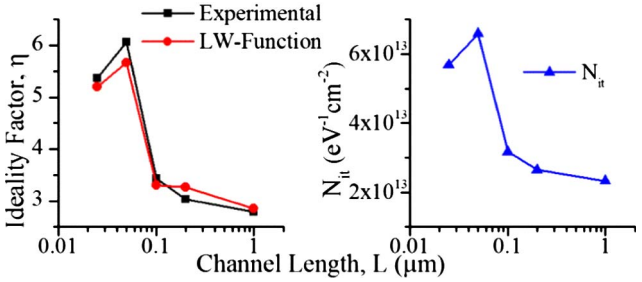

Fig. 5. Variation of η extracted experimentally from the maximum sub-threshold slope (black lines) and from LW-Function (red lines) and N_{it} with L. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

fundamental differences of the two methods. The ideality factor obtained from the LW function methodology is in very good agreement with the one directly deduced from the maximum sub-threshold slope (see Fig. 5). The fast interface trap density can be deduced from the ideality factor as indicated in the following equation:

$$N_{it} = \frac{C_{ox}}{q}\cdot(\eta-1) \tag{5}$$

The values extracted are in the range 3×10^{13}–6×10^{13}/eV/cm^2. Additionally, from the θ_1-G_m slope we found the series resistance equal to $R_{SD}\approx 310\,\Omega\,\mu m$, which is a reasonably good value for such UTB III–V devices.

Concerning the saturation region, examples of typical I_d-V_g characteristics (symbols) measured at $V_d = 1$ V are presented in Fig. 6 both in linear and logarithmic scale for channel lengths L = 1 μm and 0.2 μm. In [7] the MOSFET drain current compact model based on the Lambert-W function (Eq. (2)) has been extended in all operation regimes. We applied this model (Eqs. 6–10) to the devices under test, using v_{sat} and DIBL as fitting parameters while keeping the extracted values from the linear region for the other parameters (V_t, η, μ_0, R_{SD}).

$$I_d = \frac{I_{d,0}}{1+g_{m,0}\cdot\left(R_{s,eff}+\frac{R_{SD}}{2}\right)+g_{d,0}\cdot R_{SD}} \tag{6}$$

where

$$I_{d,0} = \frac{\beta}{C_{ox}\cdot V_d}\left[\frac{\eta kT}{C_{ox}}\cdot\left[\frac{1}{2\cdot\eta kT}\cdot Q_{i|V_d=0}^2 + C_{ox}\cdot Q_{i|V_d=0} - \frac{1}{2\cdot\eta kT}\cdot Q_i^2 + C_{ox}\cdot Q_i\right]\right] \tag{7}$$

$$Q_i(V_g + DIBL\cdot V_d, V_d, V_t, \eta) = \frac{\eta kT}{q}C_{ox}\cdot LW\left(e^{q\cdot\frac{(V_g+DIBL\cdot V_d)-V_t-V_d}{\eta kT}}\right) \tag{8}$$

$$R_{s,eff} = \frac{1}{W\cdot C_{ox}\cdot v_{sat}} \tag{9}$$