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Silicon tunnel FET with average subthreshold slope of 55 mV/dec at low drain currents

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ABSTRACT

In this paper we present a silicon tunnel FET based on line-tunneling to achieve better subthreshold performance. The fabricated device shows an on-current of $I_{on} = 2.55 \times 10^{-7}$ A/μm at $V_{ds} = V_{on} = V_{gs} - V_{off} = -0.5$ V for an $I_{off} = 1$ nA/μm and an average SS of 55 mV/dec over two orders of magnitude of I_d. Furthermore, the analog figures of merit have been calculated and show that the transconductance efficiency g_m/I_d beats the MOSFET performance at low currents.

1. Introduction

Tunnel FETs (TFETs) are promising candidates to overcome MOSFETs subthreshold slope (SS) limit of 60 mV/dec for low power computing and internet of things applications. Unlike MOSFETs which rely on thermionic emission of electrons or holes over a barrier, TFETs exploit quantum band to band tunneling of carriers through source to channel. This effect has less dependence on temperature and also filters out high and low energy tails of the Fermi distribution of carriers leading to steeper switching slopes [1]. Experimental demonstrations of TFETs using different materials have been already published [2,3]. Among these materials silicon TFETs show the best I_{on}/I_{off} ratio [4], while having less on-current I_{on} compared to TFETs with III-V due to its indirect large bandgap. However, one of the huge advantages of silicon TFETs is that they are compatible with conventional CMOS fabrication processes which allows for advanced device designs and complementary circuits, as already demonstrated by Complementary-TFET inverters [5,6]. Moreover, different architectures of TFETs like planar, tri-gate and gate all around (GAA) Si nanowires have been reported [7,8]. GAA geometry greatly improves the gate electrostatic control over source-channel tunneling junction which leads to improvements in average SS, I_{on}/I_{off} ratio and analogue characteristics like conductance and transconductance. Despite these improvements, Silicon TFETs, like other TFETs still suffer from degraded SS which can be attributed to improper dopant distribution profile and Trap Assisted Tunneling (TAT). The latter contributes to premature thermionic increase of current before actual BTBT process begins, while the former leads to longer tunneling distance which in turn decreases tunneling probabilities and subthreshold slope (SS). Implantation into silicide (IIS) and low temperature annealing [9] were proposed as a solution to dopant profile optimization at the tunneling junction.

In this paper, we take a novel approach to take advantage of line tunneling with source-gate overlap to improve the subthreshold slope and I_{on} of devices. Conventional point tunneling takes place at p-i or n-i junction, while in devices with source-gate overlap, provided with enough band bending, line tunneling occurs from the source to semiconductor-oxide interface (Fig. 1(a and b)). It has been shown that line-tunneling can achieve steeper SS [10]. However, in a real device both of these contributions are present as depicted in Fig. 1(c). We take advantage of line-tunneling, as shown in Fig. 2, by first implantation and spike annealing using a dummy gate, and then etching down the source area to remove the end of range (EOR) implantation damage to reduce possible TAT and importantly to increase the electric field in the thinner area for line-tunneling with respect to the thicker part of the device where point-tunneling happens.

2. Device fabrication

TFET devices as illustrated in Fig. 2 were fabricated on a 20 nm SOI wafer with 145 nm buried oxide as starting substrate. First, PECVD SiO_2

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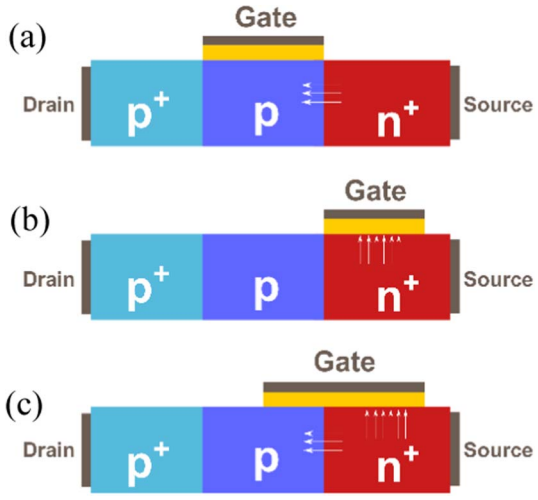

Fig. 1. pTFET device configuration. (a) Tunneling path of carriers in case of point-tunneling, where tunneling occurs at the source channel interface. (b) Tunneling path of carriers in case of line-tunneling where the tunneling takes place in the gate/source overlapped region with a direction parallel to the gate electrical field. By applying a gate voltage a depletion/inversion region beneath the gate is formed and carriers tunnel to the oxide interface. (c) In a real device, both tunneling types contribute to the current.

was deposited and patterned to form the dummy gate. Then implantations of boron and phosphorus ions followed by high temperature spike annealing at 1050 °C were carried out to form the source and drain regions. Phosphorous was implanted with two different implantation doses of $2 \times 10^{14}\,cm^{-2}$ and $2 \times 10^{15}\,cm^{-2}$ to compare resulting devices. It should be noted that for each implantation step, the other side of the device was covered by photoresist to avoid intermixing of dopants. TRIM simulation of implantation for phosphorous in Fig. 3(a) shows that EOR damages reside at around 10 nm depth, indicating the importance of thinning down source area to less than 10 nm. The TCAD simulated dopant profile after annealing (Fig. 3(b)) further indicates an active dopant concentration of $3 \times 10^{19}\,cm^{-3}$ for a dose of $2 \times 10^{14}\,cm^{-2}$ at a depth of 15 nm, corresponding to a source thickness of 5 nm after thinning down as described below. After annealing, the dummy gate was removed and 60 nm PECVD SiO_2 was deposited and patterned to open a window for thinning down the source junction. Source was etched down to 5 nm at room temperature by wet etching. Afterwards, 3 nm of ALD HfO_2 and 60 nm of PVD TiN were deposited and patterned to form the High-k/Metal Gate stack. 2 nm of Ni was deposited and annealed at 750 °C for 30 s to form $NiSi_2$ with smooth interface and low resistivity [11]. Fig. 2 schematically summarizes the key process steps.

3. Experimental results

3.1. Transfer characteristics

Fig. 4(a) presents the I_d-V_g transfer characteristics of the fabricated pTFET device with 2 µm channel length and 2 µm gate width for a 1.5 keV phosphorus implantation dose of $2 \times 10^{14}\,cm^{-2}$ at source which after activation corresponds to a dopant concentration of $3 \times 10^{19}\,cm^{-3}$ at 5 nm thickness based on process simulations (Fig. 3(b)). Thenceforth we name this device T1. The device T1 shows steep increase of current with an average SS of 55 mV/dec over two decades of I_d current between 10^{-13} to 1.5×10^{-11} A/µm at $V_d = -0.1$ V which is superior the state of the art GAA silicon nanowire pTEFTs with an average SS > 60 mV/dec [7]. Furthermore, the I_{on}/I_{off} ratio is about 2.55×10^2 at $V_{ds} = V_{on} = V_{gs} - V_{off} = -0.5$ V for $I_{off} = 1$ nA/µm. Fig. 4(b) shows a hump in the SS vs I_d plot which divides the transfer curve into two parts. To explain the hump Fig. 5 depicts different tunneling regions and mechanisms in our device. Line-tunneling occurs in two distinct regions, one region over the thinned source and other region over the thicker part of the device especially stronger at the top corner owing to the fringing field. To investigate in detail, TCAD simulation with Sentaurus was carried out. Models for fermi statistics, drift-diffusion transport, doping dependent SRH generation-recombination and non-local BTBT have been self-consistently solved with the Poisson equation for the structure. Parameters for the high-k dielectric and silicon were taken from the standard library of the TCAD software. Fig. 6(a) shows the simulated transfer characteristics of the device at $V_d = -0.3$ V. At $V_g = -0.1$ V line-tunneling initially starts at the top corner as a result of fringing field induced tunneling and then extends on the ramp due to contribution of E_t and E_R as indicated in Fig. 6(b). Increasing V_g to -1 V causes the line tunneling in the thinner area as shown by the contour of band to band generation in Fig. 6(c). This further increases the current but gives rise to the hump in the characteristics.

Fig. 7(a) shows the transfer characteristics of a pTFET with a higher source implantation dose of $2 \times 10^{15}\,cm^{-2}$ at 1.5 keV energy, which hereafter is called T2. Due to higher doping concentration the fringing field induced tunneling starts at an earlier voltage resulting in onset-voltage shift of 0.25 V. On the other hand, a higher voltage V_g is required to form a depletion region for line-tunneling at the thin area of the source in the device T2 owing to the higher doping concentration. This also results in a hump which is clearly visible in SS vs I_d plot for transistor T2 in Fig. 7(b) but occurs at a higher voltage compared to transistor T1. The hump in the transfer characteristics appears at $V_g = -0.09$ V for T1 whereas it appears at higher voltage of $V_g = -0.21$ V for T2 as a result of higher doping concentration.

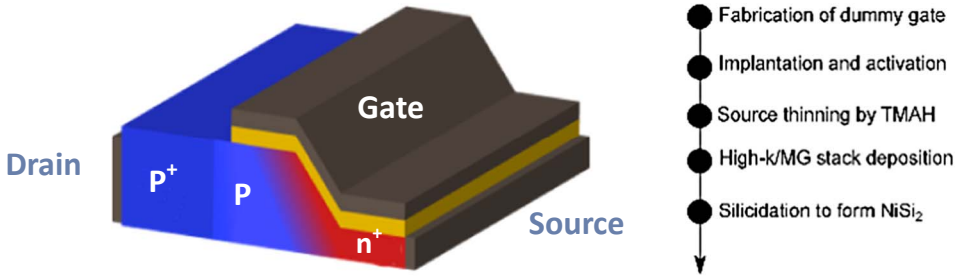

Fig. 2. Fabrication schematics and key process steps. After implantation and activation, the source is thinned down through wet etching to get rid of EOR damages.