Solid State Electronics xxx (xxxx) xxx–xxx

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Role of AlGaN/GaN interface traps on negative threshold voltage shift in AlGaN/GaN HEMT

Amit Malik*, Chandan Sharma, Robert Laishram, Rajesh Kumar Bag, Dipendra Singh Rawal, Seema Vinayak, Rajesh Kumar Sharma

Solid State Physics Laboratory (DRDO), Timarpur, Delhi 110054, India

ARTICLE INFO

The review of this paper was arranged by Prof. E. Calleja

Keywords:
AlGaN/GaN HEMT
Interface states
Reverse gate bias stress
TCAD ATLAS simulation
Threshold-Voltage Shift

ABSTRACT

This article reports negative shift in the threshold-voltage in AlGaN/GaN high electron mobility transistor (HEMT) with application of reverse gate bias stress. The device is biased in strong pinch-off and low drain to source voltage condition for a fixed time duration (reverse gate bias stress), followed by measurement of transfer characteristics. Negative threshold voltage shift after application of reverse gate bias stress indicates the presence of more carriers in channel as compared to the unstressed condition. We propose the presence of AlGaN/GaN interface states to be the reason of negative threshold voltage shift, and developed a process to electrically characterize AlGaN/GaN interface states. We verified the results with Technology Computer Aided Design (TCAD) ATLAS simulation and got a good match with experimental measurements.

1. Introduction

Trap states plays an important role in AlGaN/GaN HEMT device performance. Donor like surface states is believed to be responsible for formation of two dimensional electron gas at AlGaN/GaN interface even without any intentional doping [1,2]. There are also many disadvantages associated with different type of traps in HEMT structures. RF dispersion, gate lag, drain lag, kink effect are some of the undesirable effects of traps [3–5]. So it is very important to identify the location and type of traps present in device and their effect on various device characteristics. Traps in AlGaN/GaN HEMT also influence the threshold voltage of the device [6]. Stability of threshold voltage is very important for reliability and safety of HEMT devices [7]. So it is very important to understand the shift of threshold voltage and traps responsible for the threshold voltage shift.

The interface states at Insulator layer and semiconductor is proposed to be the reason for the threshold voltage shift after reverse gate bias stress in MIS HEMT [6–9]. To the best of our knowledge, there is no reported study on reverse gate bias stress induced negative shift in threshold voltage of AlGaN/GaN HEMT and their relation with AlGaN/GaN interface states.

In this paper, we report an experimental study of change in threshold voltage to a higher negative voltage after application of reverse gate bias stress of fixed time duration. This negative shift in threshold voltage is proposed to be caused by de-trapping of electrons from AlGaN/GaN interface states to the channel during reverse gate bias stress. A simple method to extract the interface states density at AlGaN/GaN interface and their characteristics time constant from measured electrical characteristics is developed. The hypothesis is confirmed by TCAD ATLAS simulation study that shows a close match with experimental results.

2. Experiment details

2.1. HEMT device fabrication

The devices are fabricated on HEMT epi-structure grown by in-house Metal Organic Chemical Vapor Deposition (MOCVD) system on 3″ SiC substrate. Epi-layer structure includes AlN nucleation layer over SiC substrate, 2.5 μm GaN layer, 1 nm AlN spacer layer, 24 nm thick $Al_{0.23}Ga_{0.77}N$ barrier layer and 1 nm GaN cap layer. Mesa isolation is achieved by Cl_2/BCl_3 based inductively coupled plasma reactive ion etching (ICP RIE) [10]. Ohmic contacts are formed by Ti/Al/Ni/Au metal scheme, followed by rapid thermal annealing. Schottky gate contacts are made by Ni/Au metal stack. Passivation layer of about 100 nm SiN is deposited after gate formation using plasma enhanced chemical vapor deposition (PECVD). Source to drain spacing is 4 μm, gate length is 0.75 μm and gate width is 100 μm.

* Corresponding author.
E-mail address: amitspl09@gmail.com (A. Malik).

https://doi.org/10.1016/j.sse.2018.01.002
Received 21 September 2017; Received in revised form 6 December 2017; Accepted 15 January 2018

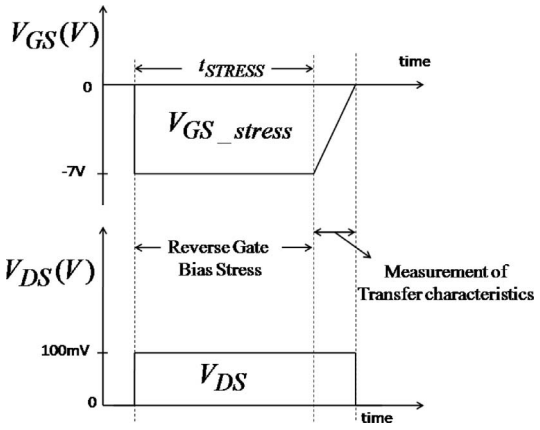

Fig. 1. Biasing condition of HEMT during application of reverse gate bias stress followed by measurement of Transfer characteristics.

2.2. Measurements

All the measurements reported are carried out using Agilent B1500A parametric analyzer. Measurements are performed at low Source to drain voltages (V_{DS}) to avoid self-heating effects. To check for reverse gate bias stress induced threshold voltage shift transfer characteristics of the device are measured before and after application of reverse gate bias stress (as shown in Fig. 1). The transfer characteristics are measured at V_{DS} = 100 mV by varying the gate to source voltage (V_{GS}) from 0 V to −7 V. The device is then biased in reverse gate bias stress condition at $V_{GS\,stress}$ = -7V and V_{DS} = 100 mV for a time duration of 15 s (hold time), followed by measurement of transfer characteristics by varying V_{GS} from −7 V to 0 V. Stress time duration (t_{stress}) of 15 s is chosen to best showcase the maximum threshold voltage shift.

In both measurements V_{GS} is varied in steps of 0.05 V and at each bias step the measured drain current is average of current values in 3.3 ms time duration (medium integration time of parametric analyzer B1500A). Experimentally measured results are shown in Fig. 2(a). The threshold voltage before off-state stress is around V_T = −3.6 V and after the application of off-state stress for 15 s, threshold voltage shifts (ΔV_T) by about −0.5 V reducing V_T to −4.1 V.

So the measured characteristics clearly depicts negative shift in threshold voltage after application of reverse gate bias stress on HEMT device.

3. Proposed model

3.1. Theoretical treatment

Threshold voltage of AlGaN/GaN HEMT device can be approximated as [11]

$$V_T(t) \approx -qn_s(t)/C_g \quad (1)$$

where q is electronic charge, n_s is two dimension electron carriers concentration below the gate and C_g is gate capacitance per cm^2. Threshold voltage is directly proportional to two dimensional electron gas (2DEG) in channel. The negative shift in threshold voltage can be caused by increase in charge carrier concentration in channel below the gate after reverse gate bias stress. The shift in V_T is around 14% of unstressed value. So if the shift in V_T is caused by increase in carries due to de-trapping of electrons from some trap states during reverse gate bias stress, the net change in 2DEG (Δn_s) should be about 14% of unstressed value. The value of net change in 2DEG comes about $\Delta n_s \approx 1.1 \times 10^{12}$ cm^{-2}.

The different trap states which can affect V_T of AlGaN/GaN HEMT after reverse gate bias stress can be classified in four different categories. These are GaN bulk traps, AlGaN/GaN interface traps, AlGaN bulk traps and interface trap states at gate metal-AlGaN barrier interface. We consider the role of each of these trap categories in threshold voltage shift.

If these electrons have to come from GaN bulk the trap density should be of the order of 1×10^{19} cm^{-3}, which is unrealistically high value for GaN bulk trap density. Such a high value of GaN bulk traps density should lead to very high buffer leakage current. Fig. 3 shows the measured buffer leakage current (I_{BF}) in off-state condition (V_{GS} = −7 V). I_{BF} is calculated as

$$I_{BF} = I_S - (I_G(V_{DS} = 0\,\text{V})/2) \quad (2)$$

where

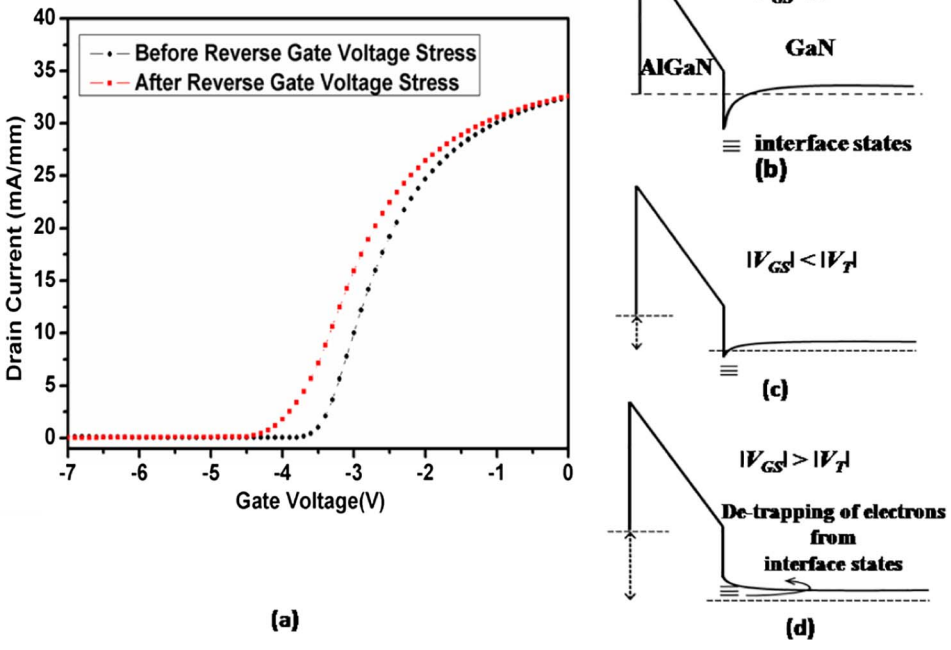

Fig. 2. (a) Transfer characteristics of device measured before and after reverse gate bias state stress at V_{GS} = −7 V and V_{DS} = 100 mV for a time duration of 15 s. Conduction band diagram of HEMT for (b) V_{GS} = 0 V, (c) $|V_{GS}| < |V_T|$ and (d) $|V_{GS}| > |V_T|$. For $|V_{GS}| > |V_T|$ electrons are de-trapping from interface states.