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Leakage current suppression with a combination of planarized gate and overlap/off-set structure in metal-induced laterally crystallized polycrystalline-silicon thin-film transistors

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ABSTRACT

A novel inverted staggered metal-induced laterally crystallized (MILC) polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) with a combination of a planarized gate and an overlap/off-set at the source-gate/drain-gate structure were fabricated and characterized. While the MILC process is advantageous for fabricating inverted staggered poly-Si TFTs, MILC TFTs reveal higher leakage current than TFTs crystallized by other processes due to their high trap density of Ni contamination. Due to this drawback, the planarized gate and overlap/off-set structure were applied to inverted staggered MILC TFTs. The proposed device shows drastic suppression of leakage current and pinning phenomenon by reducing the lateral electric field and the space-charge limited current from the gate to the drain.

1. Introduction

A great deal of attention has been given to research on poly-crystalline-silicon (poly-Si) thin-film transistors (TFTs), with investigations on the use of active matrix organic light emitting diode (AMOLED) and liquid crystal display (LCD) technology in the construction of peripheral circuits. The poly-Si reveals relatively higher field-effect mobility than that of amorphous silicon (a-Si) which is sufficiently high to operate as a driving and switching transistor in active matrix flat-panel display devices [1,2]. Thus, methods of crystallizing a-Si at low temperature have been widely applied such as solid phase crystallization (SPC), excimer laser annealing (ELA), metal-induced lateral crystallization (MILC), etc. However, the ELA, which has been widely used in the flat panel display industry using XeCl laser, is expensive and causes thermal damages to gate metal during its liquid-solid phase transformation [3,4]. SPC silicon shows relatively low field-effect mobility due to the small size and high density of grains [5,6]. Also, its high crystallization temperature and long process time could cause thermal damage on the glass substrate. Both ELA and SPC have critical problems for fabricating inverted staggered type poly-Si TFTs, while the MILC could overcome these limits due to its low process temperature of around 500 °C, high mobility from good crystallinity silicon and large grains, and less thermal damage to the gate metal and substrate [7,8]. However, the MILC TFT suffers from a relatively high off-state leakage current caused by defects in the active layer resulting from its catalytic process using Ni silicide. It has been reported that the leakage current in poly-Si TFTs arises from the high electric field between the channel and drain regions, which results in the activation of free carriers from the trap states within the grain boundary itself, although Ni-mediated crystallized poly-Si causes more trap states from Ni contamination. After the completion of the lateral growth of crystallization, the Ni silicide generally captured in the grain boundary remains in poly-Si [6,9,10]. The defects acting as a trap state induce a relatively high leakage current, due to the trapped carriers, which is easily activated from the defect energy level existing in the forbidden region [11]. This could induce a leakage current such as field-enhanced thermal excitation of trapped carriers, field-enhanced tunneling, and leakage current between the gate and the drain [12–14].

In this study, we examined a novel inverted staggered structure to alleviate this drawback. A combination of a planarized gate and an overlap/off-set structure was applied to an inverted staggered TFT that was sourced from the mechanism of a lightly doped drain (LDD) and field-induced drain (FID) structure, reported to be effective for reducing leakage current [15–17]. Shifting the position of the etch-stopper to the direction of the drain side could create an undoped Si area between the channel and drain that does not on the influence of gate bias. Moreover, the planarized gate structure provides thicker gate dielectric to reduce the space-charge limited current (SCLC) than inverted staggered structure of protruded gate when the position of the etch-stopper is modified. Therefore, the suggested TFT could reduce the activation of

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the carrier from the lowered lateral electric field on the drain side and the leakage current from the gate to the drain.

2. Experimental details

In this work, we produced a novel structure of TFT modified from an inverted staggered TFT widely used in industry. First, we deposited a 100 nm-thick buffer silicon oxide on a glass substrate (Corning eagle XG, $10^5 \times 10^5$ mm^2) in a plasma-enhanced chemical vapor deposition (PECVD) system. A 100 nm-thick $Mo_{0.9}W_{0.1}$ as an electrode layer was deposited on buffer oxide by a direct current magnetron sputtering system and etched in an aluminum etchant (H_3PO_4 + CH_3COOH + H_2O). Then, a 500 nm-thick silicon oxide was deposited on the electrode layer. To make silicon oxide trench, the thick silicon oxide layer was patterned to form the same shape as that of the electrode layer using self-aligned back-side exposure with negative photo-resist (PR) and etched using reactive ion etching (RIE) system. The trench was filled with Ni and Cu. Ni as an adhesion layer of 50 nm-thick was electroplated in 1 M $NiSO_4$, 0.2 M $NiCl_2$, and 0.5 M H_3BO_3 of plating bath. Cu for a gate metal by DC electroplating with acidic sulphate-plating baths, consisting of 0.1 M $CuSO_4$ and 1 M H_2SO_4. In addition, 20 μM thiourea and 300 μM HCl were used as additives for a smooth surface [18,19]. The electroplating process was advantageous for filling the trench and fabricating the planarized gate structure. After completion of the fabricated planarized gate structure, a 80 nm-thick silicon nitride was deposited in the PECVD to act as a gate dielectric with a diffusion barrier of Cu. Then, a 70 nm-thick a-Si was deposited in the PECVD system. Subsequently, silicon oxide was deposited and patterned in a buffer oxide etchant of the same size as the perpendicularly overlapping region of the channel and gate to act as an etch-stopper to prevent the damage on channel during seperation of the source and drain through RIE. To investigate the influence of the overlap/off-set structure, four other samples are fabricated by shifting the etch stopper by 1 μm and 2 μm in the direction of the source and drain, respectively. Fig. 1a and b show schematic illustrations of the planarized gate TFT and inverted staggered TFT, respectively, comparing the transformed features as the etch-stopper was shifted to the drain region from the channel area shown in Fig. 1c and d. As the position of the etch-stopper was shifted to the drain region, the source region was overlapped and the drain became off-set perpendicularly with the gate. Therefore, the influence of the gate bias decrease near the drain region, and increase at the source region. Then, extrinsic silicon (p^+) was deposited by PECVD and etched to segregate the source and the drain region by RIE. After the completion of all deposition processes, the extrinsic and intrinsic silicon layers were defined to the source, channel, and drain in the RIE system. Then, the gate dielectric was etched by in-situ RIE process. After that, MILC process was carried out in vacuum ambient to generate poly-Si [20]. Finally, dopants were activated and dangling bonds were passivated simultaneously during furnace annealing in H_2 ambient for 2.5 h. For comparison, the conventional inverted staggered TFTs were also processed under the same conditions, except the process fabricating the gate structure.

3. Results and discussion

The transfer characteristics (I_D-V_G curves) of normal planarized gate MILC TFT were examined with the gate bias swept in the gate voltage range from -20 to 10 V at the −1 V of fixed drain bias (Fig. 2). These curves reveal that the TFT exhibits good electrical characteristics including high on-current, low off-current, low subthreshold slope and a high field-effect mobility of 69.3 cm^2 V^{-1} s^{-1}. However, the planarized gate TFT still denotes a sharp increase of current in the positive gate bias region related to the trapped carriers in the high electric field due to Ni silicide defects in channel/drain junction. In the MILC process, $NiSi_2$ migrates toward the a-Si region, leaving crystallized silicon behind the trace. When the $NiSi_2$ moving forward at the front collides

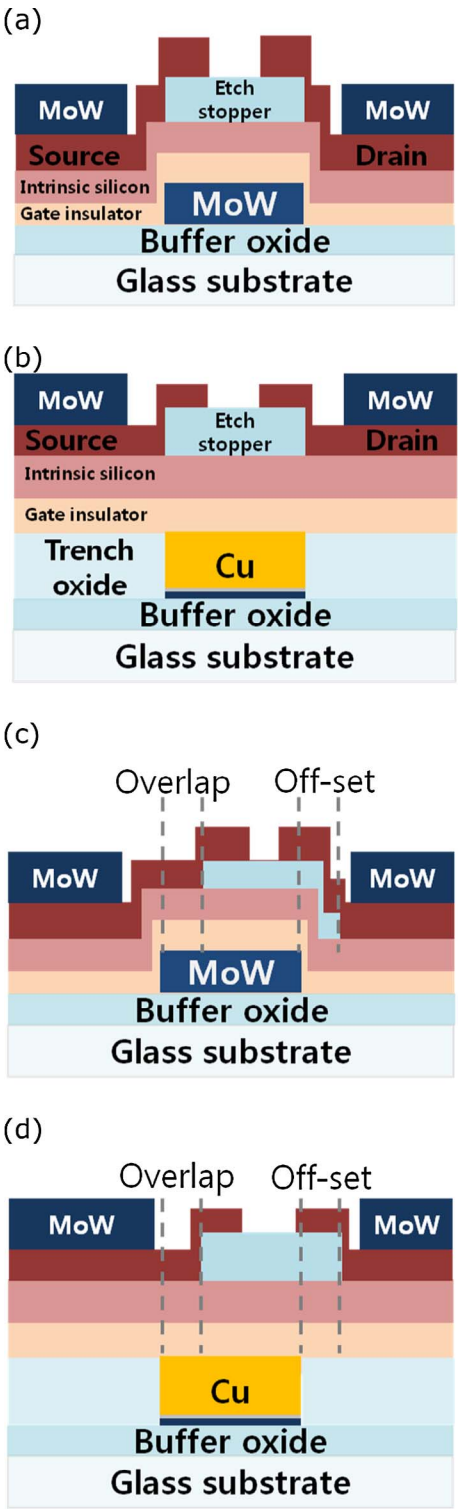

Fig. 1. Schematic cross-sectional view of (a) inverted staggered TFT, (b) planarized gate TFT, (c) inverted staggered TFT with drain off-set structure was applied, and (d) planarized gate TFT with drain off-set structure was applied.

with the already crystallized silicon, the $NiSi_2$ becomes captured between the poly-Si grains. Then, Ni silicide captured at the grain boundary generates high density of charge trapping states in the forbidden band-gap region [10,11]. These charge trap states are related to leakage current resulting from the thermionic emission due to the thermal excitation of trapped carriers occurring in the low gate bias region as well as to the field-enhanced tunneling of the trapped carriers