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Compact modeling of nanoscale triple-gate junctionless transistors covering drift-diffusion to quasi-ballistic carrier transport

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ABSTRACT

In this work, we extend our analytical compact model for nanoscale junctionless triple-gate (JL TG) MOSFETs, capturing carrier transport from drift-diffusion to quasi-ballistic regime. This is based on a simple formulation of the low-field mobility extracted from experimental data using the Y-function method, taking into account the ballistic carrier motion and an increased carrier scattering in process-induced defects near the source/drain regions. The case of a Schottky junction in non-ideal ohmic contact at the drain side was also taken into account by modifying the threshold voltage and ideality factor of the JL transistor. The model is validated with experimental data for n-channel JL TG MOSFETs with channel length varying from 95 down to 25 nm. It can be easily implemented as a compact model for use in Spice circuit simulators.

1. Introduction

Junctionless (JL) multi-gate transistors with high doping concentration within the channel and the source/drain regions have been proposed, simplifying the source/drain engineering by removing the related p-n junctions [1,2]. Compared to the junction-based multi-gate transistors they offer higher on-state current, lower off-state current, near ideal subthreshold slope and very small drain-induced barrier lowering (DIBL) due to the screening effect of the surrounding gate and the absence of a potential barrier at the source edge of the channel when the transistor operates in the on-state [1–5]. With channel dimensions scaling, the carrier transport in JL transistors becomes increasingly ballistic due to absence of carrier reflection at the source/channel junction and increase of the injection carrier velocity [6,7]. It has been demonstrated that the degree of ballisticity in JL nanowires above threshold increases with increasing the device cross-section through reduced phonon scattering [6].

The ballistic transport has been modeled by Monte Carlo simulation and deterministic sub-band Boltzmann approach [8] or by quantum transport [9]. Based on the effective mobility extracted from the potential distribution along the channel from Monte Carlo simulations, the ballistic mobility has been evaluated from the effective mobility and the long channel mobility using Matthiessen's rule [10]. Calibration of the ballistic mobility from the linear to the saturation region provided a way to extend drift-diffusion (DD) simulation into the era of Si FinFETs and NWs down to 2 nm design rules [10]. A physics-based model capturing carrier transport from DD to the ballistic regime has been presented [11]. However, the model in [11] uses separate expressions for the critical length of long-channel and short-channel devices making it unsuitable for compact modeling, while it does not take into account carrier degeneracy for the injection velocity. Recently, DD compact model covering carrier transport from DD to ballistic regime has been presented by modifying the drain current expression in terms of the average charge in the channel and an effective carrier velocity accounting for the source injection velocity and the carrier degeneracy effect [12]. However, in [12] the injection velocity model includes four fitting parameters, which can be extracted by comparing it with TCAD simulations for the charge dependence of injection velocity due to the carrier degeneracy effect. For extension of the DD model to include ballistic effects, an empirical ballistic mobility model has been proposed added to the total high-field mobility according to Matthiesenn's rule [13]. This DD model has been shown to reproduce Monte Carlo linear and saturation drain currents in high mobility InGaAs FDSOI and FinFET transistors for gate lengths down to 13.5 nm [13].

More recently, we have developed a threshold voltage-based analytical DD compact model for JL triple-gate (TG) MOSFETs in the depletion regime [14]. From the analytical expression of the central potential at the conductive path, analytical expressions for the threshold voltage and subthreshold swing coefficient were derived, through which the normalized mobile charge can be determined. Using a unified

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drain current equation in terms of the unified mobile charges at the source and drain terminals, the transfer and output characteristics were reproduced with good accuracy including the short-channel effects, the saturation velocity overshoot, the series resistance and the mobility degradation effects. The observed mobility degradation with decreasing the channel length has been explained with defects induced near the source and drain regions induced by the additional implantation used to reduce the access series resistance. The impact of these defects on the device performance has been introduced considering the case of gate insulator/channel interface traps uniformly distributed along the channel [14].

To include ballistic effects in DD model, from a compact model viewpoint the channel region can be represented by a chain of DD resistors and one ballistic resistor which does not disappear for long channels (quasi-ballistic transport) and a second channel that bypasses the first one with a ballistic resistor (pure ballistic transport) [13,15]. In this work, considering that there are no electrons traveling purely ballistically in low mobility JNTs and taking interface traps of density $5 \times 10^{11}\,cm^{-2}\,eV^{-1}$ which is in line with the near ideal subthreshold slope of typical long-channel JL TG MOSFETs, we extend our DD analytical compact model to the quasi-ballistic regime by modifying the low-field mobility incorporated in the high-field effective mobility [14]. The low-field electron mobility μ in JL transistors can be reliably extracted from the slope of the Y-function $Y = I_{ds}/\sqrt{g_m}$ in the linear region ($V_{ds} = 30$ mV):

$$Y = [(W_{eff}/L)C_{ox}\mu V_{ds}]^{1/2}(V_{gs}-V_t), \quad (1)$$

where g_m is the device transconductance, V_t is the threshold voltage, C_{ox} is the gate capacitance per unit area and $W_{eff} = W_{fin} + 2H_{fin}$ is the effective nanowire width [16]. From the linear plot of the Y-function versus gate voltage V_{gs} in the depletion regime, μ is extracted from the slope of the straight line. However, in the devices of the present technology the channel doping adjacent to the contact regions is increased by the additional ion implantation, leading to an enhancement of the electron scattering and a reduction of the measured average electron mobility which is known as pocket effect [17]. The low-field mobility is formulated taking into account the ballistic motion and the increased carrier scattering near the source/drain regions due to the pocket effect [17]. Furthermore, the influence of non-ideal ohmic resistance at the drain side on the performance of short-channel JL transistors has been introduced in the compact model by modifying the distribution of the central potential at the conductive path, used to define the threshold voltage and ideality factor [14]. The modified DD compact model is validated with experimental data for long- and short-channel JL TG n-MOSFETs.

2. Extension of the drift-diffusion compact model into the ballistic regime

The measured JL TG MOSFETs were fabricated at CEA-LETI on (1 0 0) SOI wafers with 145 nm thick buried oxide [18]. After thinning Si body down to about 10 nm, a full-sheet implantation was carried out before active patterning with a phosphorus doping targeted at $2 \times 10^{19}\,cm^{-3}$. The high-k metal gate stack was composed of HfSiON/TiN/p^+-polysilicon, with an equivalent oxide thickness of 1.2 nm. An additional implantation was performed to source/drain regions with the aim of improving electrical performance by reducing access resistance, resulting in source/drain doping level $\approx 1 \times 10^{20}\,cm^{-3}$. The effective dimensions for the fin height H_{fin} and fin width W_{fin} are 10 nm and 18 nm, respectively, and the channel length L is varying from 95 to 25 nm. A schematic representation of the TG JL MOSFET is shown in Fig. 1.

The turn-on characteristics of JL TG MOSFET with L = 35 nm are presented in Fig. 2(a) for drain voltages V_{ds} = 1 V and 30 mV. The early saturation of the current at the low drain voltage indicates the presence of a Schottky junction at the drain side as demonstrated by TCAD

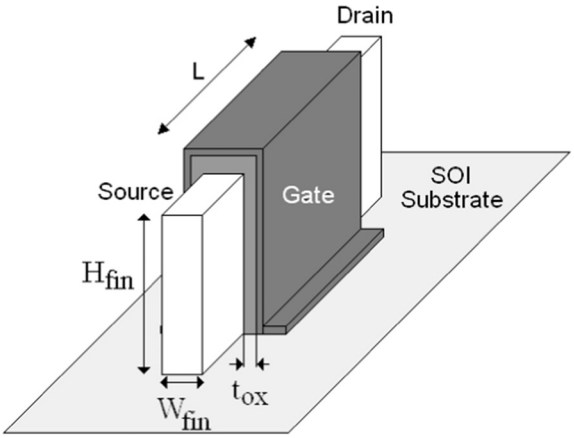

Fig. 1. Schematic representation of JL TG MOSFET.

simulations for similar behavior of the drain current in JL nanowire FETs [19]. This feature is supported with the outputs characteristics of Fig. 2(b) where the linear regions before saturation are absent as is expected for usual transport mechanism. A power-law dependence of the form $I_d \sim V_{ds}^m$ is observed before saturation in the plots of the same characteristics on log-log scale (Fig. 3). The power exponent m determined from the slope of the straight lines is m = 2.9, which is indicative of space-charged limited (SCL) current in the Schottky's junction at the drain side, in the presence of an exponential distribution of traps [20]. For similar transistor and from a different die, the transfer and output characteristics have the expected behavior for ohmic contact at the drain side as shown in Fig. 4 [19]. The output conductance g_d at different gate voltages, obtained from the experimental data of Fig. 4(b), is presented in Fig. 5. The most interesting feature of the experimental $g_d(V_{ds})$ curves in the low V_{ds} region is the decrease of g_d with decreasing V_{ds} at high gate voltage in our short-channel device, indicating the presence of a Schottky junction in the ohmic contact at the drain side [14,19]. Due to the forward bias of the Schottky junction, the barrier height increases with decreasing V_{ds}, resulting in a decrease of the output conductance. For long-channel devices (L > 50 nm), the output conductance shows a saturation behavior in the low V_{ds} region for all gate voltages (not presented), indicating that the influence of the non-linear drain resistance is negligible due to the large channel resistance compared to the total series resistance. These results show that JL TG MOSFETs suffer for large variability in contact resistance due to random dopant fluctuation and/or process control.

The transfer characteristics of JL TG MOSFETs, with drain current normalized by W_{eff}/L with $W_{eff} = 2H_{fin} + W_{fin}$, are shown in Fig. 6 for different channel lengths. With shrinking the channel length from 95 nm down to 25 nm, the threshold voltage is reduced and the ideality factor is degraded due to short-channel effects, with a simultaneous decrease of the electron mobility. Fig. 7(a) shows the corresponding plots of Y versus V_{gs} for typical JL TG MOSFETs of channel lengths L = 95, 65 and 25 nm. The Y-function method for extracting the low-field mobility has the advantage of being unaffected by the series resistance and the mobility attenuation factor. The data of μ versus L, extracted from JL transistors of ten different dies, are presented in Fig. 7(b), where two separate groups of data are observed showing a linear decrease of the mobility with decreasing the channel length. This finding reveals the occurrence of mobility variability in the JL transistors. The mobility degradation at small gate lengths may physically happen due to the process-induced defects near the source and drain regions, which has been experimentally shown to occur as the mobility degradation was found to be independent of the channel doping concentration [16]. Moreover, in nanoscale transistors ballistic motion can be an important limitation of the electron mobility, with the ballistic mobility defined in the linear region as [21]: