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Leakage Characterization of Top Select Transistor for Program Disturbance Optimization in 3D NAND Flash

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Abstract -- In order to optimize program disturbance characteristics effectively, a characterization approach that measures top select transistor (TSG) leakage from bit-line is proposed to quantify TSG leakage under program inhibit condition in 3D NAND flash memory. Based on this approach, the effect of Vth modulation of two-cell TSG on leakage is evaluated. By checking the dependence of leakage and corresponding program disturbance on upper and lower TSG Vth, this approach is validated. The optimal Vth pattern with high upper TSG Vth and low lower TSG Vth has been suggested for low leakage current and high boosted channel potential. It is found that upper TSG plays dominant role in preventing drain induced barrier lowering (DIBL) leakage from boosted channel to bit-line, while lower TSG assists to further suppress TSG leakage by providing smooth potential drop from dummy WL to edge of TSG, consequently suppressing trap assisted band-to-band tunneling current (BTBT) between dummy WL and TSG.

Keyword -- 3D NAND Flash Memory, characterization, leakage, top select transistor, program disturb.

1. Introduction

Since traditional 2D NAND Flash memory which adopts floating gate technology suffers lithography limitation, cell to cell interference and limited electrons per cell for further scaling down [1] [2], three-dimensional (3D) NAND flash memory, featuring a vertical poly-silicon channel, has become a mainstream technology for high-density mass storage devices [3-7]. However, compared with 2D NAND, it faces an inherent challenge of program disturbance due to extra program-disturbance modes and poly-silicon channel based select transistor [8] [9]. It has been found that large leakage current flowing from channel to bit-line (BL) degrades the program disturbance performance [10]. For top select transistor (TSG) of a string in 3D NAND memory, it is difficult to suppress the leakage due to complex leakage mechanisms of poly-silicon channel [11], despite a cylindrical structure.

To evaluate TSG leakage under program-inhibit situation, traditional approach measures boosted channel potentials by comparing the speed of the program cell and inhibited cell, and the difference in speeds is defined as boosted channel potential [14]. However, this method requires complicated test configuration, such as additional