Electrical Characterization of Vertically Stacked p-FET SOI Nanowires

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PII: S0038-1101(17)30732-3
DOI: https://doi.org/10.1016/j.sse.2017.12.011
Reference: SSE 7379

To appear in: *Solid-State Electronics*

Received Date: 29 September 2017
Revised Date: 4 December 2017
Accepted Date: 20 December 2017

Please cite this article as: Cardoso Paz, B., Cassé, M., Barraud, S., Reimbold, G., Vinet, M., Faynot, O., Antonio Pavanello, M., Electrical Characterization of Vertically Stacked p-FET SOI Nanowires, *Solid-State Electronics* (2017), doi: https://doi.org/10.1016/j.sse.2017.12.011

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Abstract—This work presents the performance and transport characteristics of vertically stacked p-type MOSFET SOI nanowires (NWs) with inner spacers and epitaxial growth of SiGe raised source/drain. The conventional procedure to extract the effective oxide thickness (EOT) and Shift and Ratio Method (S&R) have been adapted and validated through tridimensional numerical simulations. Electrical characterization is performed for NWs with [110]- and [100]-oriented channels, as a function of both fin width (W_{FIN}) and channel length (L). Results show a good electrostatic control and reduced short channel effects (SCE) down to 15 nm gate length, for both orientations. Effective mobility is found around two times higher for [110]- in comparison to [100]-oriented NWs due to higher holes mobility contribution in (110) plan. Improvements obtained on I_{ON}/I_{OFF} by reducing W_{FIN} are mainly due to subthreshold slope decrease, once small and none mobility increase is obtained for [110]- and [100]-oriented NWs, respectively.

Keywords—performance; transport; electrical characterization; vertically stacked nanowire; SOI MOSFET; channel orientation

I. INTRODUCTION

Once increasing the number of gates results in stronger immunity against short channel effects due to higher electrostatic coupling, triple gate (3G) and Gate-All-Around (GAA) MOSFETs attracted the interest of both scientific community and semiconductor industry [1]–[3]. Multiple gate MOSFETs with nanoscale silicon thickness and fin width, also called nanowires, have shown great performance and scalability, turning into one of the best candidates for future technological nodes [2], [4]. In these devices the silicon film thickness and the fin width are of the same order of magnitude.