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PII: S0038-1101(17)30532-4
DOI: http://dx.doi.org/10.1016/j.sse.2017.07.005
Reference: SSE 7276

To appear in: *Solid-State Electronics*

Please cite this article as: Wong, H., Yu, Q., Dong, S., Kakushima, K., Iwai, H., Geometry and Temperature Effects on the Threshold Voltage Characteristics of Silicon Nanowire MOS Transistors, *Solid-State Electronics* (2017), doi: http://dx.doi.org/10.1016/j.sse.2017.07.005

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Abstract

This work reports the observations of different geometry and temperature dependencies of electrical characteristics of silicon nanowire transistors with gate length of a couple microns. Several abnormal characteristics degradations were observed. As the gate lengths as well as the source/drain doping level of the devices under investigation were well beyond the punchthrough conditions, these observed characteristic degradations should not be due to conventional short-channel effects. We ascribed these observations to the charge transport along the corners/boundaries of the nanowires. Current enhancements were observed because of the higher mobility and larger density of states at the corners where the surface states have opposite effects on these parameters. Temperature dependence of the threshold voltage shows a linear decrease as the temperature increases. This trend is ascribed to the charge states at oxide/nanowire