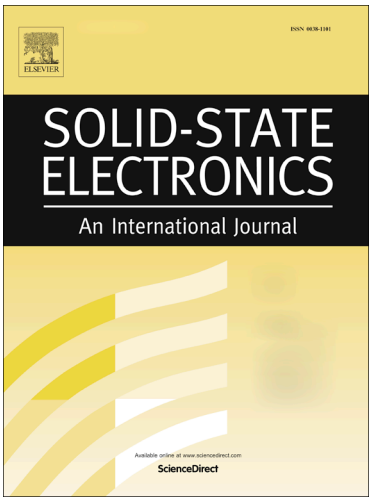

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Use DAS Algorithm to Break Through the Device Limitations of Switched-capacitor-based DAC in an ADC Consisting of Pipelined SAR and TDC

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Abstract

Switched capacitors are widely used in integrated circuits for discrete-time signal processing. Metal-Insulator-Metal (MIM) capacitors and MOSFET switches are commonly used for switched-capacitor circuits. They impose limitations in the power consumption and the bandwidth of the circuits. For instance, the switched-capacitor digital-to-analog converter (DAC) is the critical circuit block that determines the performance in a successive approximation register (SAR) analog-to-digital converters (ADC). In this paper, a design using the detect-and-skip (DAS) algorithm to break through the device limitations of switched-capacitor-based DACs is analyzed in a coarse-fine SAR ADC architecture. When it is shown that compared with the state-of-the-art Vcm-based capacitive DAC (CDAC), the DAS algorithm reduces 55% of the energy and extends the valid bandwidth from 2 MHz to 16 MHz with a 6-bit resolution under the same setting and technology. Besides, a time-to-digital converter (TDC)-assisted pipelined SAR ADC architecture using the DAS algorithm is proposed. Implemented in a 180 nm CMOS process, the 10-bit 10-MS/s prototype measures an energy efficiency of 57.8 fJ/conv.-step.

Keywords: DAS, switched capacitor, CMOS process, energy, bandwidth, CDAC, ADC, SAR, pipeline