



A review of electrical characterization techniques for ultrathin FDSOI materials and devices



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ABSTRACT

The characterization of nanosize SOI materials and devices is challenging because multiple oxides, interfaces and channels coexist. Conventional measurement methods need to be replaced, or at least updated. We review the routine techniques that proved efficient for the evaluation of bare SOI wafers (essentially the pseudo-MOSFET) and of MOS structures (transistors and gated diodes). Informative examples are selected to illustrate the typical properties of advanced SOI wafers and MOSFETs. We will show how the ultrathin film and short-channel effects affect the interpretation of the experimental data.

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1. Introduction

The future landscape of the micro-nano-electronics industry is subject of debates, strategic decisions and ... question marks. Whether the ultimate device will be FinFET [1], nanowire [2,3], planar SOI [4,5] or 3D [6] is not clear yet. The winner is expected to cumulate fast transport capability, electrostatic integrity and reliability. The old couple Si-SiO₂ is gradually giving way to more talented materials such as high-k dielectrics and strained Ge or III–V semiconductors.

Two trends are however ineluctable: the CMOS scaling will continue and, from now on to the end of the avenue, the MOS transistor will operate in fully depleted (FD) mode. Electrostatic considerations impose the body of the transistor to be sub-10 nm thick (hence FD) in at least one direction, vertical or lateral, and preferably controlled by multiple gates. An oxide underneath the body is a clear asset for dielectric isolation and back-biasing schemes.

For these reasons, we believe that the planar Semiconductor-On-Insulator technology (SOI) is the simpler solution to date. State-of-the-art SOI MOSFETs combine ultrathin strained body, thin buried oxide (BOX), short high-K/metal gates, and take advantage of substrate biasing. In these FD devices, the evaluation of basic parameters, such as carrier mobility and lifetime, threshold voltage, or oxide and interface defects, is no longer straightforward. Multi-channel coupling and thickness/length nanosize effects modify not only the measured value, but also the meaning

of classical parameters. The optimization of SOI materials, device integration modules, compact models and design libraries requires increasingly accurate characterization able to address sub-10 nm thick structures.

This paper is not aimed as an exhaustive encyclopedia of the numerous techniques and variants elaborated mainly for thick SOI materials and devices. Instead, we focus on practical methods that, according to our experience, proved to be efficient and relatively easy to implement in ultrathin films. The following section describes the generic methods for measurement and parameter extraction using as test vehicles MOS transistors and diodes. In Section 3, we discuss in detail the material evaluation and typical properties. The pseudo-MOSFET is an indisputable technique which has recently been enriched with advanced modules. It can be complemented with back-gated Hall effect and Second Harmonic Generation measurements. Section 4 is dedicated to FDSOI transistors and shows the variation of the key device parameters (threshold voltage, mobility, subthreshold slope and leakage current) with film thickness, back-bias and strain. We finally discuss the impact of short-channel effects and other scaling-related mechanisms (coupling and supercoupling, parasitic bipolar transistor, floating body). Guidelines for measurement strategies and accurate interpretation of the experimental data are suggested.

2. Characterization techniques and associated parameter extraction

The techniques selected and discussed in this section can be applied indifferently to front and/or back-gate measurements.

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For simplicity, we will refer to ‘front’ and ‘back’ channels although these notions are less and less appropriate as the SOI film becomes thinner. In ultrathin FDSOI, the carriers induced by one gate tend actually to spread in the entire film; ‘volume’ inversion/accumulation [7,8], rather than a charge-sheet surface channel, is often prevalent.

2.1. Current-based methods in MOSFETs

In advanced MOSFETs, the drain current in linear regime (low drain voltage) versus the applied voltages and the geometry of the transistor can be written as [9]:

$$I_D = \frac{W}{L} \cdot \frac{\mu_0}{1 + \theta_1 \cdot (V_G - V_T) + \theta_2 \cdot (V_G - V_T)^2} \cdot C_{OX} \cdot (V_G - V_T) \cdot V_D \quad (1)$$

where W and L are the width and the length of the transistor, μ_0 is the low-field mobility, V_G and V_D are the applied voltages on the gate and on the drain, V_T is the threshold voltage, and θ_1 and θ_2 are the mobility attenuation factors due to series resistance and surface roughness, respectively.

I_D - V_G curves are measured, for a given V_D , with the aim of extracting the parameters V_T and μ_0 , based on Eq. (1). The non-linear dependence of I_D versus V_G requires specific treatment. We will describe the usual methods (Y-function, double derivative and McLarty) as well as their application conditions in the next sections.

2.1.1. Y-function method

This method is widely used for the transistors in which the θ_2 term is negligible, i.e. the vertical electric field in the channel is sufficiently low, such as the surface roughness does not play an important role in the mobility reduction. In this configuration, I_D in Eq. (1), and the associated transconductance, g_m , can be written as:

$$I_D = \frac{W}{L} \cdot \frac{\mu_0}{1 + \theta_1 \cdot (V_G - V_T)} \cdot C_{OX} \cdot (V_G - V_T) \cdot V_D \quad (2)$$

$$g_m = \frac{dI_D}{dV_G} = \frac{W}{L} \cdot \frac{\mu_0}{[1 + \theta_1 \cdot (V_G - V_T)]^2} \cdot C_{OX} \cdot V_D \quad (3)$$

The direct use of these two equations is not practical due to the non-linearity induced by θ_1 factor. The Y-function, defined to eliminate θ_1 [10], is straightforward to apply:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L}} \cdot \mu_0 \cdot C_{OX} \cdot V_D \cdot (V_G - V_T) \quad (4)$$

After the channel formation ($V_G > V_T$), Y has a linear dependence versus V_G (see Fig. 2a for MOSFET and Fig. 17 for pseudo-MOS). Its intercept with the V_G -axis yields the threshold voltage, while the slope gives the low-field mobility. Coefficient θ_1 is determined from the slope of $1/\sqrt{g_m}(V_G)$ line. Since $\theta_1 \approx R_{SD} \cdot \mu_0 \cdot C_{OX} \cdot W/L$, the series resistance R_{SD} can be evaluated.

Note that this simple method is effective for fully fabricated MOSFETs, as well as for pseudo-MOSFET. The limitations are related to the hypothesis of negligible impact of surface roughness on the mobility. Practically, after tracing the Y-function versus the gate voltage, the linearity of the curve indicates the appropriateness of this method.

2.1.2. Double derivative

The second derivative method was developed to eliminate the dependence on the series resistances that induces inaccuracy in the threshold voltage extraction. Additionally, this extraction technique is not affected by the mobility degradation [11,12]. The

threshold voltage is the gate voltage corresponding to the peak of the transconductance derivative, i.e., the second derivative of the drain current (Fig. 1). In FDSOI devices, the peak of the second derivative of front-channel $I_D(V_{G1})$ characteristics yields the front threshold voltage for different conditions at the back interface. When the front and the back channels are activated (Fig. 1b), the second derivative curve exhibits two peaks [13–15].

The main drawback of this method comes from the high sensitivity to measurement errors and noise. Indeed, the use of the second derivative data treatment leads numerically to a high-pass filter [11]. The $I_D(V_G)$ measurements should be performed with very small steps ($\Delta V_G < 10$ mV). The threshold voltage detected by the second derivative corresponds qualitatively to the one provided by the first derivative of the gate capacitance-voltage characteristics (see also Section 2.3.3).

2.1.3. McLarty method

In order to account for surface roughness effects, which increase rapidly with vertical field, the simple formulation of the effective mobility in Eq. (2) needs to be enriched as in Eq. (1):

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1(V_G - V_T) + \theta_2(V_G - V_T)^2} \quad (5)$$

The second mobility attenuation factor θ_2 can lead to a negative transconductance at high V_G ; its physical meaning is explained in [16]. Whether θ_2 is important or not can be deduced by drawing the Y-function. If $Y(V_G)$ plot is linear, θ_2 can be safely ignored. When θ_2 is relevant, it leads to an upturn of the $Y(V_G)$ plot, as shown in Fig. 2a and expressed by:

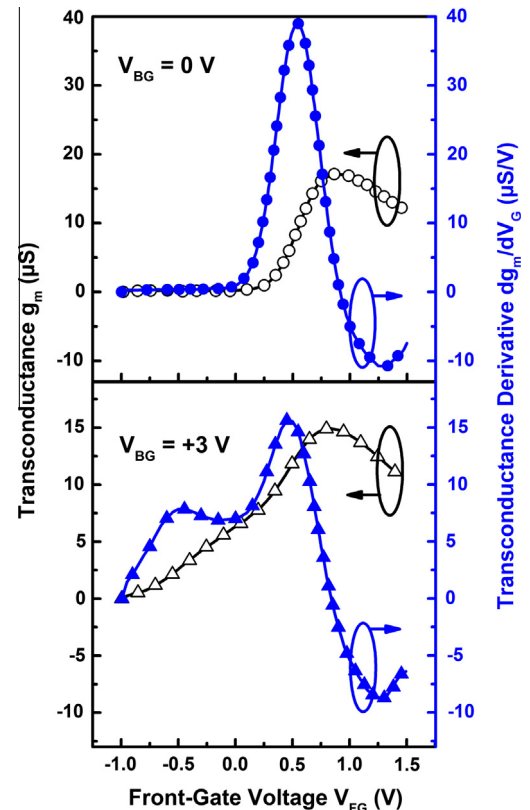


Fig. 1. Transconductance and transconductance derivative versus front-gate voltage. (a) $V_{BG} = 0$ V: the peak indicates the threshold voltage. (b) $V_{BG} = +3$ V: the two peaks show the consecutive activation of the back channel (for $V_{FG} = -0.5$ V) and front channel (for $V_{FG} = +0.5$ V).

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