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Letter

A sharp-switching device with free surface and buried gates based on band modulation and feedback mechanisms

Y. Solaro [a,b], P. Fonteneau [a], C.A. Legrand [a], C. Fenouillet-Beranger [c], P. Ferrari [b], S. Cristoloveanu [b,*]

[a] STMicroelectronics, 850 Rue Jean Monnet, F-38926 Crolles Cedex, France
[b] IMEP-LAHC, Grenoble Institute of Technology, Minatec, France
[c] CEA-LETI MINATEC Campus, France

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ABSTRACT

We propose and demonstrate experimentally a band-modulation device with extremely sharp switching capability. The Z^3-FET (Zero gate, Zero swing and Zero impact ionization) has no top gate, is processed with FDSOI CMOS technology, and makes use of two adjacent buried ground planes acting as back gates. The buried gates emulate respectively N^+ and P^+ regions in the undoped body, forming a virtual thyristor-like NPNP structure with feedback operation. Vertical output I_A–V_A and transfer I_A–V_G characteristics over more than 8 decades of current are measured with relatively low gate and drain bias (<3 V).

1. Introduction

The increased demand for low-power electronics has accelerated the quest of sharp-switching devices, prompting a variety of concepts. Superlattice nanowire FETs [1] and Landau-switch devices with air–gap suspended gate [2,3] or ferroelectric dielectric stack [4,5] are still at the theoretical/simulation level, with hypothetical chances for rapid adoption by industry. Progress in Tunnel FETs (TFETs) is constant albeit there is still concern about the possibility to achieve simultaneously a subthreshold swing below 60 mV/decade (fundamental limit of conventional MOSFETs) and a high ON-current [6–10].

A recent family of devices, based on band modulation and feedback mechanisms [11–20], is attracting attention thanks to their compatibility with FDSOI CMOS process. The Field Effect Diode (FED, Fig. 1a) features two adjacent top gates $G_{1,2}$ [11–14]. The Z^2-FET (Zero subthreshold swing and Zero impact ionization, see Fig. 1b) has simplified configuration, with gate G_2 being replaced by the back (substrate) contact [16–20]. The principle of operation is similar. The lateral PIN diode is forward biased but the current is blocked by two potential barriers induced by the gates: $V_{G2} < 0$ prevents the injection of electrons from the N^+ contact (cathode) and $V_{G1} > 0$ inhibits the hole injection from the P^+ terminal (anode). When V_{G1} is slightly reduced, the corresponding barrier is marginally lowered and a few holes can flow to cathode where they lower the electron barrier. Now few electrons can escape to the anode and further lower its barrier enabling more holes to be injected. This positive feedback mechanism results in sharp switching from low current (OFF state) to a high current (ON state). Since the barriers are collapsed, the ON current is high, being governed by the size of the PIN diode.

The feedback can also be triggered by increasing the drain bias. These devices may look as lateral PNPN thyristors but with important differences: (i) the body being undoped, the N and P bases of the intrinsic bipolar transistors are 'electrostatically' doped via gate field effect, (ii) there is no need of impact ionization for encroaching the two bases such as to trigger the device in ON state.

A number of pragmatic applications have been documented: capacitorless single-transistor dynamic memory (1T-DRAM) [14,17,18], protection device against electrostatic discharge (ESD) [12,13,19,20], surface-charge ion sensor [15], etc. The capacitance between the two top gates may impact the performance of the FED at high-frequency (Fig. 1a). This problem is alleviated in Z^2-FET (Fig. 1b), where one of the front gates is avoided and the gate-underlapped region of the body remains available for sensing

* Corresponding author.

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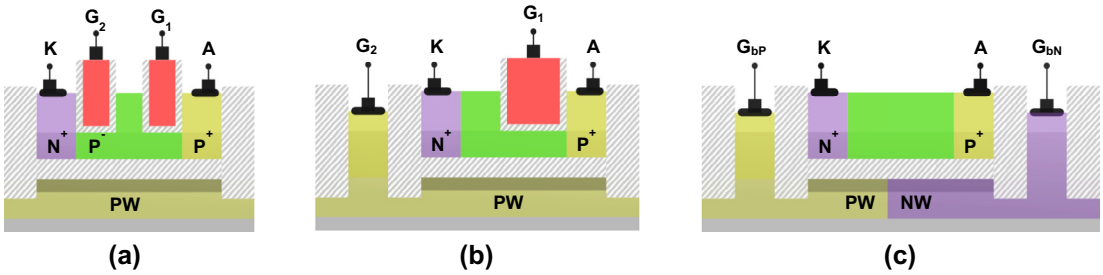

Fig. 1. Configuration of (a) FED [11–14], (b) Z^2-FET [16–20], and (c) Z^3-FET proposed in this paper.

applications. In this letter, we propose and document another version of band modulation device with simplified architecture and totally free surface.

2. Z^3-FET principles and processing

In order to eliminate the top gates and related contacts, we introduce the Zero-gate version (Z^3-FET) illustrated in Fig. 1c. This novel device is constructed using the standard design rules of the FDSOI technology. Ground planes underneath a thin buried oxide (BOX) are a natural option since they already serve to tune the threshold voltage of CMOS circuits. We use two side-by-side ground planes which received P^+ and N^+ doping and operate as back gates ($G_{bP,N}$ in Fig. 1c). The device configuration can also be regarded as an upside-down FED [11–14].

The following are details of the CMOS process. We used SOI wafers (from SOITEC) with thin BOX (25 nm) and ultrathin (~10 nm), undoped Si film. The film thickness has been completed by epitaxial growth to reach t_{si} = 24 nm, which is the usual thickness of raised regions for source and drain. N/P-wells and corresponding N^+/P^+ ground planes have been formed by deep implantation underneath the BOX (Fig. 1c). The ground planes are heavily doped such as to prevent any depletion effect at BOX-substrate interface. Lateral GP contacts, formed by local opening of the BOX, were located outside the STI-isolated body. The CMOS steps related to the deposition and anneal of the high-k/metal gate stack were omitted notably simplifying the process. Instead, a protection oxide has been deposited on the surface.

The absence of the conventional ultrathin gate dielectric is a remarkable advantage in terms of reliability issues for Z^3-FETs operated at high voltage. Replacing the top gate stacks with buried ground-planes transfers the reliability concern to the BOX which is sufficiently thick and can withstand much higher breakdown voltage.

The left bottom gate G_{bP} (Fig. 1c) controls the body region near the cathode by inducing a virtual P-type doping; it can be negatively biased or simply grounded because the workfunction difference is sufficient to build up the N^+/P^+ injection barrier between cathode and body. The second bottom gate G_{bN} plays a reciprocal role on the anode side: it is positively biased such as to emulate N^+ body doping. The placement and the biasing of the two ground-planes was selected to form adequate injection barriers while maintaining the buried N^+/P^+ diode underneath the BOX in reverse mode for low leakage current.

3. Z^3-FET characteristics

Measurements were performed with various biases on anode and ground planes. Typical output characteristics $I_A(V_A)$ are reproduced in Fig. 2a. At low anode voltage, the diode is blocked and the leakage current is remarkably low (I_{leak} < 10 fA/μm). Increasing V_A reduces the difference ($V_{GbN} - V_A$) and gradually lowers the barrier on the anode side until the feedback mechanism is triggered. A very sharp transition to the ON-state region is observed: the anode current switches by 8 decades or more for a very small increase of V_A ($\Delta V_A \sim 1$ mV) around the turn-on voltage. The ON current is high (>10 mA) and reflects the double-injection mechanism typical in forward-biased PIN diodes.

A higher back-gate bias V_{GbN} reinforces the anode barrier, hence increased V_A is needed to collapse it. Fig. 2b shows the linear relation between back-gate bias and turn-on voltage (defined as V_A yielding I_A = 10 nA). The coupling ratio is close to one ($\Delta V_T/\Delta V_{GbN}$ = 0.9 V/V) thanks to the relatively thin BOX. It follows that the turn-on voltage can easily be tuned between 0.9 V and 2.6 V according to the application envisioned. Additional flexibility for optimizing the device performance and operating range is available with a negative V_{GbP} bias that reinforces the second barrier at the cathode.

Device turn-off occurs at a lower voltage V_A, when the injection barriers are fully restored. For backward sweep, the curves measured for variable V_{GbN} from 0 to +3 V are all superposed. The hysteresis window is clearly enlarged for higher V_{GbN}. This hysteresis and quasi-vertical current variation actually result from an S-shaped negative-resistance characteristic that is measurable with the TLP (Transmission Line Pulse) technique [20,21], as shown in Fig. 3a. At low current density, the snapback (S-shape, see inset) characteristic is observed. For 100 ns pulses, the triggering voltage is V_{t1} = 1.27 V and the hold voltage is V_H = 1.01 V. When the pulse duration and rise time are shortened, V_{t1} is slightly reduced (to 1.07 V). This is attributed to the triggering dependence on dV/dt [22]: the faster the voltage change, the higher the displacement current from the junction capacitances, and the earlier the device turn-on. The failure current is high (I_{t2} = 6.4 mA/μm for 100 ns pulses), showing excellent ESD performance compared to other FDSOI devices fabricated with ultrathin technology [20]. For shorter pulses (5 ns), I_{t2} is further increased and reaches 9.7 mA/μm.

The transfer characteristics $I_A(V_{GbP})$ are equally sharp with a remarkable subthreshold swing $\Delta V_{GbP}/\Delta I_A$ below 10 mV/decade, between $10^{-11} < I_A < 10^{-5}$ A/μm (Fig. 3b). However, since the Z^3-FET is operated from the back gate, the switch is less abrupt than in Z^2-FET with thin gate oxide (~1 mV/decade [16–20]). The curves can be shifted laterally by modifying V_{GbN} and V_A. Furthermore, when the difference $V_{GbN} - V_A$ is higher, the injection barrier at the anode side becomes stronger. As a result the leakage current is reduced by 4 orders of magnitude whereas the turn-on voltage is marginally increased (Fig. 3b). When the second ground plane is operated, the $I_A(V_{GbN})$ curves show symmetric behavior with those in Fig. 3b: sharp increase in current, from OFF-state (V_{GbN} > +1 V) to ON-state (V_{GbN} < +1 V), modulated by V_A and V_{GbP}.

Numerical simulations reveal the size effects and optimization trends. For the injection barriers to be fully efficient, a minimum barrier length $L_{N,P}$ should be maintained which limits the scaling