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Letter

High-performance logic transistor DC benchmarking toward 7 nm technology-node between III–V and Si tri-gate n-MOSFETs using virtual-source injection velocity model

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ABSTRACT

Injection velocity (v_{inj}) is a unique figure-of-merit that determines logic transistor ON-current (I_{ON}) and switching delay (CV/I). This paper reports on Virtual-Source (VS) based analytical and physical model, which was calibrated by using state-of-the-art experimental data on III–V and Si tri-gate n-MOSFET, aiming to compare High-Performance (HP) logic transistor performance at 7 nm technology-node. We find that a significant increase in the virtual source injection velocity and improvement in the electrostatic integrity are critical, to meet the projected I_{ON}/I_{OFF} ratio for the 7 nm technology node.

1. Introduction

Multi-gate transistor architectures were successfully introduced at the 22 nm technology node to improve the electrostatic integrity of the device [1]. However, for further geometry scaling and performance improvement, the use of high mobility channel materials, such as III–V and Ge, seem to be critical at the 7 nm technology-node and/or beyond [2,3]. Consistent with strategies for Si CMOS scaling, III–V FETs with non-planar architecture, such as III–V FinFETs, are likely to be a very attractive candidate in the context of performance, electrostatic integrity, and V_{DD} scaling. In this paper, we try to use state-of-the-art experimental data on III–V and Si tri-gate n-MOSFET to construct the VS model, aiming to carrying out High-Performance (HP) logic device benchmarking, targeting at the 7 nm technology-node. This approach can accurately predict an ON-current (I_{ON}) parameter, since the model relies on the measured data and realistic projection of critical device parameters, such as injection velocity (v_{inj}), threshold voltage (V_t), series-resistance ($R_{sd} = R_s + R_d$), inversion capacitance (C_{inv}) and power supply voltage (V_{DD}), while possessing acceptable electrostatic criteria, such as I_{OFF} = 100 nA/μm @ $V_{DS} = V_{DD}$ V and V_{GS} = 0 V).

2. Virtual-Source (VS) modeling

2.1. VS modeling for state-of-the-art Tri-gate Si and InGaAs MOSFETs

For accurate benchmarking between Si and III–V devices at 7 nm technology-node, it is highly desirable to build a model, based on state-of-the-art L_g = 30–34 nm Si tri-gate n-MOSFETs [1] and L_g = 60 nm $In_{0.53}Ga_{0.47}As$ tri-gate n-MOSFET [2]. At its heart, we constructed a charge-based model for the I–V characteristics of Si and III–V tri-gate n-MOSFETs, based on the Virtual-Source (VS) concept [4]. For ultra short-channel III–V devices, a direct source-to-drain tunneling (SDT) leakage current is likely to matter, which deteriorates the subthreshold-swing (SS) [5,6]. Nonetheless, we have ignored the effect of the direct SDT, since there are lack of experimental data that numerically describes the exact portion of the direct SDT leakage current yet. In addition, when L_g approaches to 10 nm and below, it is reported that v_{inj} at the top of the potential barrier (ToB) is different from v_{inj} at the VS point [7]. As a result, both velocities would show a significant difference as L_g scales down aggressively. In this regard, the beauty of our approach is in that the velocity comes directly from the experimental data and its reasonable projection with L_g.

The VS model requires several device parameters, such as C_{inv}, SS, DIBL, threshold voltage (V_t), R_s and R_d. In addition, there are two fitted parameters, such as effective mobility (μ_{eff}) and the virtual-source injection velocity (v_{inj}). Eq. (1) describes a drain current (I_D) density per unit gate width (W) from the VS perspective:

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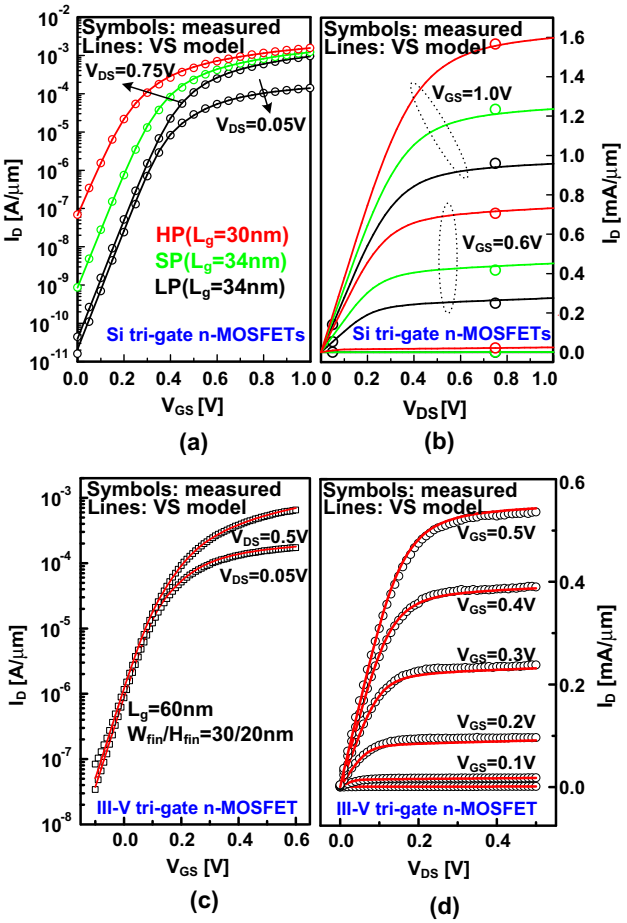

Fig. 1. (a) I_D–V_{GS} and (b) I_D–V_{DS} measured data (symbols) of Si tri-gate n-MOSFETs [1] (HP: high-performance, SP: standard-performance, LP: low-power) and their virtual-source-velocity modeling results (lines) at the given bias. In Si, only HP modeling data were used for benchmarking. (c) I_D–V_{GS} and (d) I_D–V_{DS} measured data (symbols) and VS modeling results (lines) for L_g = 60 nm III–V tri-gate nMOSFET [2].

$$I_D/w = Q_{inv} v_{inj} F_s = C_{inv}\eta\phi_t \ln\left(1+\exp\frac{V'_{GS}-(V_t-\alpha\phi_t F_f)}{\eta\phi_t}\right) v_{inj} F_s \quad (1)$$

Here, Q_{inv} is a channel charge density at the top of the potential barrier, v_{inj} is an injection velocity, F_s is a carrier velocity saturation function, C_{inv} is an effective gate-to-channel capacitance per unit area, η is a subthreshold coefficient, ϕ_t is a thermal voltage, $V'_{GS} = V_{GS} - I_D R_s$, α is a fitting parameter, and F_f is an inversion transition function. According to [4], the VS model requires six measured device parameters: C_{inv}, subthreshold-swing, DIBL, I_{OFF} @ V_{GS} = 0 V at low and high V_{DS}, total resistance @ V_{DS} = 0 V and $V_{GS} = V_{DD}$, and channel length (L_g). In addition, the model requires three additional physical fitting parameters: effective mobility (μ_{eff}), virtual-source injection velocity (v_{inj}), R_s and R_d. More details on the VS model can be found in [4].

Fig. 1 compares experimental and modeled subthreshold and output characteristics for both Si tri-gate n-MOSFETs [1] and $In_{0.53}Ga_{0.47}As$ tri-gate n-MOSFETs [2], in which the VS model yields an excellent agreement with experimental data using physically meaningful device model parameters, such as v_{inj} and μ_{eff}. The extracted key model parameters, such as C_{inv}, WR_{sd}, and v_{inj}, are summarized in Table 1 (gray boxes). Of course, C_{inv} is a strong function of gate bias. As a result, it is more appropriate to estimate the channel charge density (Q_{xo}) by integrating the C_{inv} with V_{GS}. In the strong inversion region, however, it is still reasonable to estimate the Q_{xo} by using Eq. (2).

$$Q_{xo} = C_{inv} \times [V_{GS} - V_T] \quad (2)$$

In this paper, we do not consider the gate fringe capacitance yet, since our main focus is on the channel current density (I_D). However, it will be necessary to properly model and include the fringe capacitance for high-frequency and switching simulations.

We used these model parameters as a reference to predict the performance of Si and InGaAs MOSFETs targeting at 7 nm technology-node. In particular, an interfacial-state density (D_{it}) is a critical device metric which degrades SS, especially in III–V MOSFETs [8]. First, we extracted D_{it} from InGaAs MOSCAP experimental data by using conductance method, and extracted D_{it} value was as low as 2.6×10^{12} cm^{-2} eV^{-1} [9]. In our model, the SS degradation due to D_{it} was fully included via subthreshold coefficient (η) [8].

2.2. Benchmarking of high-performance logic transistor: III–V vs. Si

In order to do a realistic benchmarking at 7 nm technology-node, first we attempt to precisely choose values of all the relevant model

Table 1
Model parameters extracted from VS modeling of experimental devices (reference in gray boxes) and interpolated model parameters between reference and L_g = 10 nm, which assume best performance parameters at each III–V and Si-channel material.

L_g of III-V	60 nm [2]	30 nm	20 nm	10 nm
V_{DD} [V]	0.5	0.75	0.67	0.59[11]
WR_{sd} [Ωμm]	202	143	124	104[11]
C_{inv} [fF/μm^2] @V_{GS}=V_{DD}	10.1	16.8	19.0	21.2[11]
v_{inj} [x10^7 cm/s]	2 @V_{DD}=0.5V	2.33	2.67	3/3.5/4[12] @V_{DD}=0.5V
μ_{eff} [cm^2/Vs]	1273	690	495	300
V_t@V_{DS}=0.05 V	0.18	0.288	0.298	0.306
L_g of Si	**60 nm**	**30 nm [1]**	**20 nm**	**10 nm**
V_{DD} [V]	-	0.75	0.67	0.59[11]
WR_{sd} [Ωμm]	-	150	127	104[11]
C_{inv} [fF/μm^2] @V_{GS}=V_{DD}	-	28.6	32.5	36.3[11]
v_{inj} [x10^7 cm/s]	-	0.92	1.13	1.35 @V_{DD}=1V[13]
μ_{eff} [cm^2/Vs]	-	124	100	76
V_t@V_{DS}=0.05 V	-	0.29	0.30	0.31