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Gamma and proton irradiation effects and thermal stability of electrical characteristics of metal-oxide-silicon capacitors with atomic layer deposited Al_2O_3 dielectric

J.M. Rafí [a,*], G. Pellegrini [a], V. Fadeyev [b], Z. Galloway [b], H.F.-W. Sadrozinski [b], M. Christophersen [c], B.F. Phlips [c], D. Lynn [d], J. Kierstead [d], M. Hoeferkamp [e], I. Gorelov [e], P. Palni [e], R. Wang [e], S. Seidel [e]

[a] Instituto de Microelectrónica de Barcelona, IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain
[b] Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, CA, USA
[c] U.S. Naval Research Laboratory, Washington DC, USA
[d] Physics Dept., Brookhaven National Laboratory, Upton, NY, USA
[e] Dept. of Physics and Astronomy, Univ. of New Mexico, Albuquerque, NM, USA

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ABSTRACT

The radiation hardness and thermal stability of the electrical characteristics of atomic layer deposited Al_2O_3 layers to be used as passivation films for silicon radiation detectors with slim edges are investigated. To directly measure the interface charge and to evaluate its change with the ionizing dose, metal-oxide-silicon (MOS) capacitors implementing differently processed Al_2O_3 layers were fabricated on p-type silicon substrates. Qualitatively similar results are obtained for degradation of capacitance–voltage and current–voltage characteristics under gamma and proton irradiations up to equivalent doses of 30 Mrad and 21.07 Mrad, respectively. While similar negative charge densities are initially extracted for all non-irradiated capacitors, superior radiation hardness is obtained for MOS structures with alumina layers grown with H_2O instead of O_3 as oxidant precursor. Competing effects between radiation-induced positive charge trapping and hydrogen release from the H_2O-grown Al_2O_3 layers may explain their higher radiation resistance. Finally, irradiated and non-irradiated MOS capacitors with differently processed Al_2O_3 layers have been subjected to thermal treatments in air at temperatures ranging between 100 °C and 200 °C and the thermal stability of their electrical characteristics has been evaluated. Partial recovery of the gamma-induced degradation has been noticed for O_3-grown MOS structures. This can be explained by a trapped holes emission process, for which an activation energy of 1.38 ± 0.15 eV has been extracted.

1. Introduction

In recent years, a number of high permittivity (high-*k*) dielectrics have been investigated for a wide range of micro/nanotechnology applications, Al_2O_3 being amongst the most studied ones [1,2]. The requirements of large area uniformity, conformality, accurate thickness control of the dielectric layers and low-temperature budget can be achieved by means of atomic layer deposition (ALD) technique. Interestingly, as a difference to other conventional thermally grown or deposited dielectrics like SiO_2 and Si_3N_4, for which positive fixed charge densities are generally obtained, intrinsic negative charges are found for ALD Al_2O_3 films [3]. The ultimate origin of the negative charges in Al_2O_3 films is still under debate, however, it has been pointed that aluminum vacancies and oxygen interstitials produce levels in the lower half of Al_2O_3 bandgap, which are candidates to trap negative charges [4,5]. These defect states may be charged by electron tunneling from Si substrate into Al_2O_3. It has been demonstrated that the presence of a SiO_2 interlayer between Si and Al_2O_3 plays a key role in negative charge formation. An increase in SiO_2 interlayer thickness is known to decrease the effective negative charge densities, eventually leading to positive charge densities for SiO_2 interlayer thicknesses in the range of 5–10 nm [6]. This has been attributed to a reduction of tunneling of electrons into SiO_2/Al_2O_3 negative traps, as well as to the introduction of fixed and bulk positive charges at the Si/SiO_2 interface and SiO_2, respectively [6].

In the last years, excellent surface passivation properties for Al_2O_3 layers on high-efficiency crystalline silicon solar cells have been proven by a considerable number of studies [7,8]. Passivation

* Corresponding author. Tel.: +34 93 5947700x2201.
E-mail address: jm.rafi@csic.es (J.M. Rafí).

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is partly attributed to the electric field induced by the negative charges, which repels charge carriers from the silicon cell surface, thus avoiding their recombination [3]. Additionally, a chemical passivation mechanism is associated with the reduction of surface recombination by a low Si/Al_2O_3 interface defect density [5]. Optimal passivation results have been obtained for Al_2O_3 layers with thicknesses typically in the range of 20–30 nm [3,5,7], while lower properties have been appreciated for thinner layers (<10 nm), what has been attributed to a reduced passivation at the Si/Al_2O_3 interface [5].

More recently, in the field of silicon tracking detectors for high-energy physics experiments, interest has also arisen for ALD Al_2O_3 passivation layers. Silicon tracking detectors are key sub-systems of any modern particle physics experiment. They provide charge particle tracking with high spatial resolution, and are capable of operating in harsh radiation environments [9,10]. Building a full size system in a large experiment, such as ATLAS [11] and CMS at CERN, is a challenging endeavor, due to the practical aspects of instrumenting large area with hermetic coverage. Typically sensors contain inactive regions at their periphery, which requires either tiling them to achieve the hermeticity, or introduction of additional layers to compensate for the acceptance gaps. There are similar requirements in other fields (e.g. medical imaging) that would benefit from maximizing sensor's active area fraction. As a part of the ATLAS Upgrade R&D, we are developing technologies for minimizing the inactive area at the periphery of the sensors, so called "slim edge" approach, to enable hermetic tiling of sensors into large instrumented areas. The method of choice in our investigation is scribe–cleave–passivate (SCP) [12]. Scribing and cleaving steps result in high surface quality on the sidewall, with low defect density [13,14]. The passivation with proper interface charge repels the carriers from the sidewall effectively achieving a resistive surface [15]. This is analogous to the voltage drop along the top surface in the guard ring region of a single-sided sensor, where a certain distance is required to sustain a given bias voltage [16]. In the SCP method the sidewall takes the role of the top region allowing the voltage gradient on its surface. For p-type bulk devices we need to use alumina (Al_2O_3) to passivate the sidewall and to provide negative interface charge with silicon, so that minority charge carriers are repelled and surface recombination is reduced. Radiation tests on such devices indicated relatively low radiation resistance for low fluences [17] with protons, but not with neutrons, indicating possible surface damage.

In recent years, a lot of work has been devoted to physical and electrical characterization of high-*k* dielectrics, as well as to reliability issues [18]. However, much less is known about their behavior in radiation environments. Different works have been published on radiation effects on a limited number of high-*k* dielectrics, with Al_2O_3 amongst them [19–22]. However, these have been mostly limited to irradiations with X-rays, electrons or heavy ions, and separated studies addressing either capacitance–voltage (*C*–*V*) or current–voltage (*I*–*V*) characterization have been generally considered. Moreover, little is known about annealing of radiation-induced damage in ALD Al_2O_3 dielectric films [23], the thermal stability of their electrical characteristics being of particular interest.

In this work, we are specifically addressing the radiation hardness of the alumina layer with ionizing radiation. To directly measure the interface charge and to evaluate its change with the ionizing dose, we manufactured Metal-Oxide-Silicon (MOS) capacitors. We varied some details of the Al_2O_3 layers processing sequence, including the use of H_2O or O_3 as oxidant precursors, film thickness and post-processing annealing. We then irradiated the different sample categories with gammas and protons and studied the effects on the electrical characteristics, as well as their thermal stability. The results indicate that some of the processing variations can produce radiation-hard alumina layers.

2. Experimental details

2.1. Al_2O_3 MOS capacitors fabrication

MOS capacitors were fabricated in Centro Nacional de Microelectrónica (CNM) cleanroom on four 100 mm-diameter (100)-oriented Czochralski-grown p-type silicon wafers with 0.1–1.4 Ω cm resistivity. After cleaning in H_2O_2/H_2SO_4 and a dip in HF (5%), a wet thermal oxidation process at 1100 °C in a quartz tube furnace resulted in a 400 nm-thick SiO_2 layer, which was patterned by photolithography and wet etching. In order to investigate any possible process-related radiation hardness differences, blanket Al_2O_3 dielectric layers with nominal thickness of 20 nm and 40 nm were deposited by ALD in two different facilities, CNM and U.S. Naval Research Laboratory (NRL) (Table 1).

Deposition of CNM Al_2O_3 layers was carried out immediately after cleaning in H_2O_2/H_2SO_4 and a dip in HF (5%). The films were deposited at 250 °C in a Cambridge NanoTech Savannah 200 system, by using trimethylaluminum (TMA) and O_3 as precursors, and N_2 as carrier and purge gas. For CNM layers O_3 was chosen as oxidant precursor, so as to reduce possible blistering phenomena. Al_2O_3 layer blistering is associated with a local delamination of the film and is thought to be caused by gaseous desorption upon thermal treatments of the ALD layers, where the dielectric films may act as a gas barrier, thus giving rise to bubble formation [5,24]. Blistering may be encountered for relatively thick (>10 nm) Al_2O_3 ALD layers and it has been found to be reduced when using O_3 oxidant instead of H_2O [25].

For the case of NRL samples, an additional Silox Vapox III etch of about 20 s was carried out, so as to remove any possible native oxide formed during handling and shipping of the wafers from CNM to NRL. Subsequently, ALD was quickly performed (within 1 min, load-lock and applying vacuum to minimize oxidation in air). NRL Al_2O_3 layers were deposited at 300 °C in an Oxford Plasma ALD system, by using trimethylaluminum (TMA) and H_2O as precursors, and N_2 as carrier and purge gas. A post-deposition anneal (PDA) treatment of 10 min at 300 °C in H_2 atmosphere was carried out for NRL wafers, just after ALD.

The Al_2O_3 film thickness was measured prior to gate formation by means of a Rudolph Research Auto EL Ellipsometer, using an index of refraction of 1.64, as well as by a Nanometrics Nanospec 6100 interferometer. The obtained physical thickness values are given in Table 1. A 500 nm-thick Al (99.5%)/Cu (0.5%) layer was deposited as the metal gate of the MOS capacitors. After patterning the metal layer by photolithography and wet etching, the back of the wafers was fully metalized with a 500 nm-thick Al layer for electrically contacting the silicon substrate. Finally, the wafers were cut into halves and one half underwent a forming gas (N_2/(10%) H_2) post-metallization annealing (PMA) step at 350 °C for 30 min. The fabricated MOS capacitors are square-shaped with five different surface areas (*A*) ranging from 9.6×10^{-3} cm^2 to 6.4×10^{-5} cm^2. No blistering phenomena were observed on neither CNM nor NRL Al_2O_3 MOS capacitors subjected or not to the PMA treatment. If the contrary is not indicated, MOS structures with 2.3×10^{-3} cm^2 and 6.4×10^{-5} cm^2 areas were used for *C*–V and *I*–*V* measurements, respectively.

2.2. Irradiation and electrical characterization

MOS capacitors were subjected to unbiased gamma and proton irradiations (the gates of capacitors were left floating) at room temperature. While gamma irradiations were carried out at