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Thin-films and transistors of p-ZnTe

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ABSTRACT

In this article, we report (I_{DS}–V_{DS}) characteristics of (75 and 35 nm) p-type ZnTe thin-film transistors (TFTs) at different active channels by photolithography. In 75 nm p-ZnTe TFTs, the source and drain contacts were doped with Cu in 11, 13 and 15 mg ($Cu(NO_3)_2$–$3H_2O$)/150 ml (H_2O) for 60 s and heated at 300 °C for 10 min. TFTs immersed in 15 mg solution showed the clearest linear and saturation regions, as well as an approximate mobility from 10^{-2} to 10^{-4} cm^2/V s. Also, drain- currents (I_{DS}) from 10^{-8} to $\sim 10^{-7}$ A were shown at $V_G = 0$ V (OFF-state). However, drain-current in the OFF-state decreased in 35 nm p-ZnTe TFTs. The films showed the cubic phase and the $Cu_{1.44}Te$-like orthorhombic phase.

1. Introduction

Amorphous silicon thin-film transistors (a-Si:H TFTs) are the devices used in Liquid Crystal Displays (LCD) and are competing against the crystalline silicon (c-Si) technology with new classes of applications that cannot be feasible by c-Si CMOS and low-cost fabrication [1–3]. Since 1973, there have been constant efforts in searching for new II–VI chalcogenide type of TFTs to improve performance or decrease the production costs of Si-based [4,5]. A wide range of II–VI semiconductors and dielectric materials can be used to make TFTs. Also, these transistors can be fabricated over rigid or flexible substrates without using monocrystalline silicon wafers, and we can obtain low or high mobility depending on materials, structure, and process. With the exception of CdTe (n and p type), the rest of the materials of the II–VI group show only one conductivity type (n or p-type), but not both. However, difficulties in accomplishing efficient doping wide-band-gap II–VI compounds of both p- and/or n-type still remain obstacles in applications [6]. This is known as self-compensation by spontaneously generated oppositely charged native defects and this limits the application of these semiconductors solely to unipolar (p-type) devices, restricting the fabrication of complementary metal oxide semiconductor (CMOS) devices, etc. [7–11]. In this group, ZnTe is the only p-type compound, due to zinc vacancy and acceptor impurities in crystal, so that the study of this material is important to fabricate complementary devices, flexible panels, etc. [12–14]. Reports of p-type TFTs are scarce, there are three recent publications that report on electrical properties of p-ZnTe TFTs [15–18]. In previous studies, we reported p-ZnTe TFTs with active channels W/L = 40/40 and 80/20 [17,18]. Here, the source and drain (S/D) bias in 75 nm p-ZnTe transistors were doped with Cu in 11, 13 and 15 mg ($Cu(NO_3)_2$–$3H_2O$)/150 ml (H_2O). Also, we calculated the mobility in (75 and 35 nm) p-ZnTe TFTs doped in 15 mg solution.

2. Experimental details

A six-step fabrication process and five masks, in combination with aligned structure, were used to fabricate (75 and 35 nm) p-ZnTe TFTs by photolithography. We deposited Au/Cr = (100/10 nm) on SiO_2/Si substrate by e-beam evaporator (Temescal 1800) to form the gate electrode with a 30 nm HfO_2 thin-film for the gate dielectric deposited by Cambridge Atomic Layer Deposition (ALD). Zinc telluride layers were synthesized by PLD at room temperature, using an excimer laser (KrF, λ = 248 nm) at energy density (E_d = 0.78 J/cm^2) with an argon partial pressure of 20 mTorr and 10 Hz of laser frecuency. 500 nm of parylene were used as a hard mask to protect the device of contamination and etch process by SCS Parylene Deposition. Then, S/D parylene contacts were removed using the Technics Series 85

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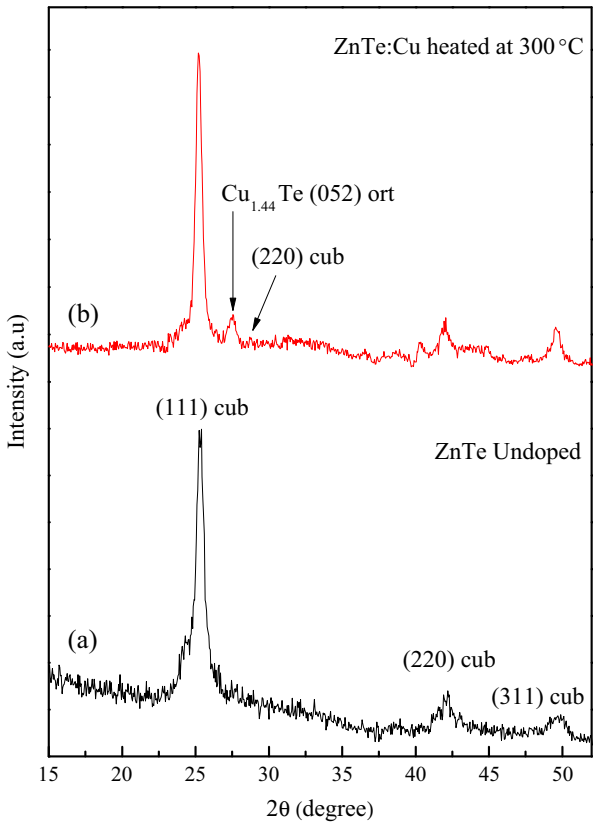

Fig. 1. X-ray diffraction patterns of ZnTe thin-films; (a) undoped films and (b) copper-doped ZnTe films heated at 300 °C for 30 min.

Table 1
Mobility of p-ZnTe TFTs at different width/length active channels.

Number of TFTs	Width, W (μm)	Length, L (μm)	Mobility, μ (cm^2/V s)
1,2	40	20	10^{-2}
3,4	40	40	10^{-2}
5,6	40	80	10^{-2}
7,8	80	20	10^{-2}
9,10	80	40	10^{-3}
11,12	80	80	10^{-3}
13,14	160	20	10^{-4}
15,16	160	40	10^{-4}
17,18	160	80	10^{-4}

Reactive Ion Etcher. The source and drain (S/D) were doped with Cu immersing the transistors in ($Cu(NO_3)_2$–$3H_2O$)/150 ml (H_2O) for 60 s. The solutions were kept at a temperature of 60 °C. Then, the TFTs were heated at 300 °C for 10 min with an N_2 atmosphere (Thermco MiniBrute). Finally, we deposited Au/Ni (100/10 nm) for the S/D contacts. For the experiments, and knowing the condition where the transistors work, we fabricated 75 nm ZnTe TFTs (W/L = 40/20) and we doped the (S/D) bias with Cu in 11, 13 and 15 mg ($Cu(NO_3)_2$–$3H_2O$)/150 ml (H_2O). Before depositing the contacts of Source and Drain, the bias on the p-type channel are open and the rest of the channel was protected with parylene. At that time we dip the TFT in the Cu-solution and only the bias was doped. Subsequently, we deposit the Source and Drain contacts, this in order to have a good ohmic contact between the semiconductor and the contacts, since there is a small contact specific resistance doping with copper. Also, we built 75 nm ZnTe TFTs immersed in 15 mg to calculate the mobility at different W/L channels (W/L = 40/20, 40/40, 40/80; 80/20, 80/40, 80/80 and 160/20, 160/40, 160/80). Mobility was calculated using the saturation region. To know the behavior of the electrical properties of TFTs, we built (35 nm) p-ZnTe TFTs (W/L = 40/40, 80/40 and 160/40) doped in 15 mg solution. The I_D–V_D characteristics were measured by probe station, CASCADE microtech. For all the experiments we applied gate voltages from 0 to −10 V with steps of −2.5 V. The structures of the films were studied by X-ray diffraction (XRD) using Cu Kα (λ) = 1.54 Å, operated at 40 kV and 44 mA.

3. Results and discussion

3.1. X-ray diffraction

Fig. 1 shows X-ray diffraction (XRD) patterns of the (a) undoped and (b) copper-doped p-ZnTe thin-films. Copper-doped was carried out immersing the ZnTe samples in 15 mg ($Cu(NO_3)_2$–$3H_2O$)/150 ml (H_2O) and then heated at 300 °C for 30 min. In Fig. 1 (a)the films show the cubic structure with X-ray peaks at 25.5°, 42°, and 49.2° corresponding to the (111), (220), and (311) planes, respectively [10]. These relative intensity X-ray peaks for the ZnTe semiconductor were compared with the JCPDS card (015-0746). The Cu1.44Te-like orthorhombic phase (052) appears when the ZnTe:Cu film was heated at 300 °C, Fig. 1(b). At this temperature, some of native copper atoms Cu° can diffuse into grains and be thermally ionized causing Cu^+ or Cu^{++}. Some ionized atoms could occupy the Zn sites in the ZnTe structure and may combine with telluride atoms [19].

3.2. ZnTe thin-film transistors

Before the construction of thin-film transistors, the p-ZnTe samples were electrically measured by circular transmission line method (CTLM) y hall effect. High resistances were obtained in undoped samples: sheet resistance ($\sim 10^{10}\ \Omega/\square$), resistivity ($\sim 10^5\ \Omega$ cm) and contact resistance ($\sim 10^6\ \Omega$) and specific contact resistance ($\sim 10^1\ \Omega\ cm^2$). These high values cause low drain current from semiconductor toward the contacts. However, these parameters drastically decreased when the films were doped with copper, especially the specific contact resistance ($\sim 10^{-4}\ \Omega\ cm^2$). This resistance means that exists good ohmic contact between semiconductor/metals. Copper-doped ZnTe films exhibit a typical p-type carrier concentration ($10^{17}\ cm^{-3}$) and Hall-effect mobility (5.98 cm^2/V s).

Fig. 1 depicts the output characteristics of (75 nm) p-ZnTe TFTs for varying Cu doping concentration, where ZnTe TFTs were immersed in (a) un-doped, (b) 11, (c) 13 and (d) 15 mg ($Cu(NO_3)_2$–$3H_2O$)/150 ml (H_2O). The active channels fabricated for this case were W/L (40/20), with gate voltage from 0 to −10 V with steps of −2.5 V. In Fig. 1(a) no switching and saturation regions can be observed at any gate voltage, due to large specific contact resistance, $\rho_c = 8\ \Omega\ cm^2$, meaning that there is not a good ohmic contact between the semiconductor and the source-drain contacts. (b) The TFT started working. However, there were overlapped curves at V_G = from −5 to −10 V. (c) A lightly saturation curves are displayed. However, in Fig. 1(d) clear linear and saturation regions are shown. This is due to low $\rho_c = 10^{-4}\ \Omega\ cm^2$ at this doped conditions, where the channel current can flow easier through ZnTe/electrode interface. For (75 nm of active layer) TFTs doped