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Effects of various gate materials on electrical degradation of a-Si:H TFT in industrial display application

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ABSTRACT

Both aluminum (Al) and copper (Cu), acting as transmission lines in the hydrogenated amorphous silicon of a thin film transistor (a-Si:H TFT), were studied to investigate electrical degradation including electron-migration (EM) and threshold voltage (V_t) stability and recovery performance. Under long-term current stress, the Cu material exhibited excellent resistance to EM properties, but a passivated SiN_x crack was observed due to fast heat conductivity. By applying electrical stress on the gate and drain for 5×10^4 s, the power-law time dependency of the threshold voltage shift (ΔV_t) indicated that the defective state creation dominated the TFT device's instability. The presence of drain stress increased the overall ΔV_t because the high longitudinal field induced impact ionization and then, enhanced hot-carrier-induced electron trapping within the gate SiN_x dielectric. An annealing effect prompted a stressed a-Si:H TFT back to virgin status. This study proposes better ΔV_t stability and excellent resistance against electron-migration in a Cu gate device which can be considered as a candidate for a transmission line on prolonged TFT applications.

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) have been intensively studied as a switching device for liquid crystal displays (LCD) during the past decade. Due to fascinating factors, such as low cost, low depositing temperature and acceptable electrical characteristics, a-Si:H TFTs are still continuously used not only on LCD glass substrate but extending their application to novel active matrix organic light-emitting diodes (AMOLED) on flexible polymer substrate and TFT driver. Although the low temperature of fabricated a-Si:H TFT has rich charge trapping sites and a defect in its interface trap as well as low electron mobility, it still possesses important advantages including large-area panel fabrication, a high breakdown field and application to standard industrial processes [1,2]. Therefore, until now, a-Si:H TFTs have been attracting much interest in realizing fundamental physics and continuously improving their electrical properties on novel devices, such as SOI TFT and gate-all-around poly-Si TFT [3,4].

In a standard TFT process, aluminum-based (Al-based) alloy is the most commonly used for gate electrodes due to its acceptable resistivity, low material cost, high adhesion on glass substrate and superior patterning ability in dry etching. However, serious electro-migration (EM) and hillock problems on Al-based alloys could induce potential open and short circuits, respectively. Therefore, copper (Cu), acting as an electrode and transmission line on TFTs, has been considered as a possible substitute for Al-based alloys due to its higher electrical conductivity and potentially greater resistance to EM failure [5,6]. Besides, the time-dependency of threshold voltage stability issues has become the most important factor affecting a-Si:H TFT performance for display panel instruments. For specific circuit designs, there are many a-Si:H TFTs that operate in both normal and reverse modes which are very susceptible to the effect of prolonged voltage stressing. Although there have been recent reports on threshold voltage shifts (ΔV_t) of a-Si:H TFTs on glass and flexible polymer substrates, most papers have mentioned that the ΔV_t could be eliminated by increasing drain voltage but illustrations of deteriorated a-Si:H TFT characteristics by thermal stress and hot-carrier-induced threshold voltage shifts during prolonged bias stress have never been reported [7–10]. In this paper, the degradation of shorter channel lengths on a-Si:H TFTs associated with various metal gate materials (Al and Cu) are extensively investigated. For the threshold voltage shift, the phenomenon of a hot-carrier generated from a high longitudinal electrical field (drain voltage), which induces more ΔV_t, will be discussed by interchanging the source and drain

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polarity. The thermal stress distribution of a TFT structure is simulated to explain the rich defect density states on the a-Si:H/SiN_x interface. For EM deterioration in both Al and Cu transmission lines, activated energy is obtained by means of long-term constant current measurement with baking at various temperatures.

2. Experimental details

Bottom-gate (BG) inverted staggered TFT with back-channel-passivated a-Si:H was used to evaluate the performances of various gate metals. The fabricated processes of this structure have been announced elsewhere [11]. Both Al and Cu metals with 150 nm thick and thin capped molybdenum acted as bottom gate electrodes was deposited on glass substrate by sputter system. The gate pattern was performed by lithography and plasma etching processes. A 400 nm thick SiN_x film and 170 nm thick a-Si:H films were sequentially deposited over metal gate for gate dielectric film and TFT channel, respectively. The thin n^+ a-Si layer was then deposited on a-Si:H surface to form ohmic contact, following by Al/Mo with thickness of 500 nm/20 nm deposition using PVD sputter chamber. The lithography and etching technologies were used to define source/drain electrodes by etching Al/Mo, n^+ a-Si layers, stop on a-Si:H channel. Finally, the passivated SiN_x layer was deposited to complete a-Si:H TFT configuration. All SiN_x dielectric and a-Si:H films were deposited in PECVD multi-chamber cluster tool. Metal films including gate electrode and source/drain of Al line were deposited by Ar+ sputter chamber. The channel width and length in this TFT devices were 36 μm and 6.5 μm, respectively. Fig. 1 depicts the schematic representation of three-dimensional industrial standard BG a-Si:H TFT structure which could be seen everywhere. Failure morphologies and element analysis were identified by field emission scanning electron microscope (FESEM, JEOL 7600F) and energy dispersive X-ray spectrometer (EDX). Meanwhile, thermal stress during various anneal conditions were simulated using the finite element analysis (FEA) software. The simulation software (ANSYS User's manual, 2010) combined with couple-field physics model of TFT device structure was calculated. Current–voltage measurement of a-Si:H TFT was performed using HP4145 semiconductor characterization system and magnetically shielding of probe station with elevating temperature stage. Based on the standard equation of long channel metal–oxide-semiconductor field-effect transistor, the threshold voltage (V_t) and field-effect mobility (μ_{FE}) could be extracted from linear and saturation regions of channel conductance [12,13]. The sub-threshold slope was derived from the inverse slope of logarithmic scale I_{ds} versus V_{gs}. According to the time-to-failure (TTF) model on micro metal lines, the activity energy of Al and Cu extracted from the Black' equation was introduced to illustrate the properties of Al and Cu signal transmission [14,15]. To evaluate the instability of the a-Si:H TFT, a bias stress of 20 V was applied to gate electrode with drain bias ranging from 0 V to 20 V. The duration of voltage bias measurement were performed up to 5×10^4 s at room temperature and interrupted at regular intervals to retrieve transfer characteristics and threshold voltage shift.

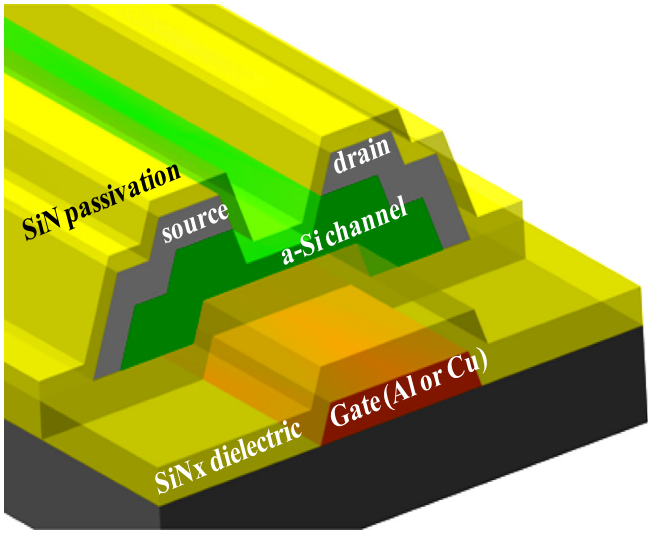

Fig. 1. Schematic depiction of bottom-gate (BG) inverted staggered structure with back-channel-passivated a-Si:H using 3D representation.

3. Results and discussion

Test structures, with 10 μm-wide and 0.43 μm-high Al/Cu metal lines capped with a Mo layer and SiN_x dielectric layer, were electrically measured to evaluate time-to-failure by constant current stress. A criterion of suddenly decreasing the current is used in defining the approximate time-to-failure (TTF) which is given by the Black equation:

$$\mathrm{TTF} = \mathrm{A}\mathrm{J}^{-n}\exp(Q/kT) \tag{1}$$

$$Q = \frac{KT_1T_2}{T_2 - T_1}\ln\left[\frac{TTF_1}{TTF_2} \times \left(\frac{J_1}{J_2}\right)^n\right] \tag{2}$$

where A is a constant, J is the current density (1×10^6 A/cm^2), n is a model parameter for the current density and takes 2 and 3 for Cu and Al, respectively. Q is the activation energy, k is the Boltzmann's constant and T is the Kelvin temperature. Under high current stress at 25 °C and 120 °C, the activation energies extracted from Eqs. (1) and (2) corresponding to the average failure time (not show here) of Cu and Al metal lines were extracted to be 0.34 eV and 0.23 eV, respectively. This elucidates that the inherently low resistivity of a Cu line is adequately used to conquer the EM issue and provide a longer life-time for signal transmission as well as gate electrodes in TFT devices. Fig. 2 shows the cross-sectional images of the failure site on both the Cu and Al lines. As shown in Fig. 2(a), a long-term current flow through the Cu line, and the Joule heating quickly spreads out over the passivated SiN_x film, consequently inducing a SiN_x crack and then, some atoms diffusing to the covered SiN_x's surface. The chemical compositions diffused from the SiN_x seams are identified. Analytical results, shown in Fig. 2(b), demonstrate that the main element of the residue on a SiN_x's surface is a Cu atom, and the inset lists the qualitative analysis of the EDX spectrum. Due to a high coefficient of thermal conductivity on the Cu material, the heating is quickly conducted into the SiN_x dielectric film, consequently inducing the SiN_x to crack, and facilitating Cu atom diffusion along the SiN_x's seams. The interface between the Cu/SiN_x dielectric-cap is the preferred failure site due to a significantly different coefficient of thermal expansion [16,17]. In Fig. 2(c), a void is found in the swelled Al line in which the failure morphology is obviously different from the Cu line. Due to a low amount of activity energy to overcome EM failure, the failure morphology of the Al line can be explained by the fact that Al atoms diffuse along the grain boundary and then, facilitate void formation [18,19]. The study concludes that the Cu material inherently proposes high activity energy to conquer the EM issue, low electrical resistivity and 30% of the coefficient of thermal expansion (CTE) which is less than that of aluminum. Although the Cu line suffers instantaneous crack failure before long-term current stress, several benefits mentioned above make Cu material the best candidate for signal transmission lines on TFT devices.

The mechanism of a thermal-induced defect creation, in terms of an increase in the density of states and the reduction of the energy barrier to break bonds in strained a-Si:H, has been qualitatively

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