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Engineering of chalcogenide materials for embedded applications of Phase Change Memory

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ABSTRACT

Phase Change Memory technology can be a real breakthrough for process cost saving and performances for embedded applications. The feasibility at 90 nm technology node has been solidly proven in an industrial environment and the added value of this solution demonstrated. Nevertheless, for specific applications some improvement in High Temperature Data Retention (HTDR) characteristics is needed. In this work we present the engineering of chalcogenide materials in order to increase the stability of RESET state as a function of temperature. This goal has been achieved by exploring Ge-rich compounds in the Ge–Sb–Te ternary diagram. In particular, an optimized $Ge_xSb_yTe_z$ Phase Change material, able to guarantee code integrity of the memory content after soldering thermal profile and data retention in extended temperature range has been obtained. Extrapolation of data retention at 10 years for temperatures higher than 150 °C cell-level has been demonstrated, thus enabling automotive applications.

1. Introduction

The competition in the embedded applications market is becoming tougher and tougher due to severe price erosion while still confirming or even enhancing performances and reliability requirements. The opportunity of wide products differentiation and specific customization can be offered by Non Volatile Memories. By keeping in mind that embedded NVM are considered a kind of "advanced option" for the CMOS platform (i.e. process architecture is CMOS driven), whose complexity will be ever increasing toward aggressive technology nodes, a storage element possibly integrated in the BEOL of the process seems the natural choice.

Aim of this paper is to propose a MOS-selected Phase Change Memory to address the NVM target for the next generation of embedded applications. The Phase Change Memory can represent a real breakthrough in terms of process cost saving and performances. It can guarantee a modular approach thanks to the integration in the BEOL of the process after contact definition. Because of the low voltage operation there is no need of dedicated devices development either for select transistor or array decoding. The PCM array can be integrated onto the CMOS platform as a real add-on offering flexibility and reliability at low additional cost. Last but not least, among all the resistive memories nowadays proposed as innovative solutions to replace Floating Gate cells, PCM is the only one ready for industrialization [1].

Nevertheless, for specific applications some improvement in High Temperature Data Retention (HTDR) characteristics of conventional material is needed. To reach this target, the engineering of chalcogenides compounds in order to increase the stability of RESET state as a function of temperature will be presented and discussed.

2. Experimental

A 90 nm 6 Metal Levels CMOS technology platform is considered as process baseline for the integration of a Wall-like Phase Change Memory [2]. The storage element is MOS-selected (Fig. 1), being this architecture the most cost effective solution for embedded applications [3]. The resulting cell area is competitive for the multi-Mb array target of embedded products, and no additional masks are needed for the integration of the select transistor. The Low Voltage one available from the CMOS platform can be effectively re-used. The chalcogenide material used to store the information is defined as a stripe (along the Bit Line direction) laying on a thin vertical heater every bit-cell. For the storage element definition 3 additional masks only are required.

The chalcogenide material is deposed by co-sputtering technique from individual targets.

In order to improve the retention properties of the PCM cell based on the Ge–Sb–Te chalcogenide, the Germanium rich portion

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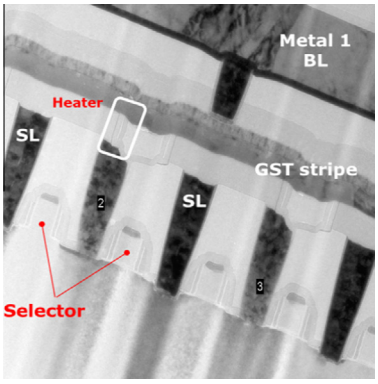

Fig. 1. A MOS-selected Phase Change Memory array: cross section along the Bit Line direction.

of the ternary diagram has been explored. In fact the conventional material, namely the $Ge_2Sb_2Te_5$ compound (GST or 225), shows a crystallization temperature close to 150 °C. In this case the metastable amorphous state is not suitable to guarantee data storage when functionality in the extended temperature range is requested by the application. For example, roughly 1–2 years high temperature data retention at 150 °C is requested in case of automotive applications. Moreover, compatibility with soldering thermal profile is needed for microcontrollers. In this case the code content is often written in the Non Volatile Memory at wafer level and must be granted till final assembly of the chip on the board. According to JEDEC standard [4] the worst case peak temperature for data retention after soldering is 2 min at 260 °C.

Several works have recently addressed the limited retention of Phase Change Memory by proposing material engineering or dopants inclusion [5–10], but no mainstream has still been found. This paper is focused on two specific compositions in the Ge-rich region, namely D-alloy and T-alloy, whose crystallization temperature is respectively 250 °C and 350 °C, so definitely higher than reference GST. The mean coordination number [11,12] is close to 3.0 in case of D-alloy and 3.5 for T-alloy. We will show that electrical performances and retention properties of Ge–Sb–Te compounds can be tailored based on the specific application. Actually there is a trade-off between SET speed and RESET retention in Ge-rich alloys, consistent with local tetrahedral Ge-Ge bonds formation [13,14], favoring a more disordered structure where the crystallization phenomenon is delayed.

3. Physical characterization

The curves of resistivity as a function of temperature have been collected for several considered alloys in the Ge–Sb–Te ternary diagram. With $Ge_2Sb_2Te_5$ as reference starting point, we moved toward the Ge-rich region, finding definitely higher values for the crystallization temperature (Fig. 2). The complementary information is related to the resistivity value of the crystalline state, since this could be a critical parameter for obtaining both a good reading window for the Non Volatile Memory and efficient programming conditions (Fig. 3). As said, by moving in the Ge-rich region, the crystallization is delayed and correspondingly the SET state appears more resistive.

Fig. 4 shows an assembly of XRD spectra of different Ge-rich alloys collected after furnace annealing at 450 °C. Crystallization into an fcc structure is observed, together with Germanium crystal segregation. This is much more evident when increasing the Germanium content, as in case of T-alloy. This is a bulk property. In the cell active volume in fact a definitely more homogenous structure is found, due to local modification of the composition induced by electrical programming [15–18].

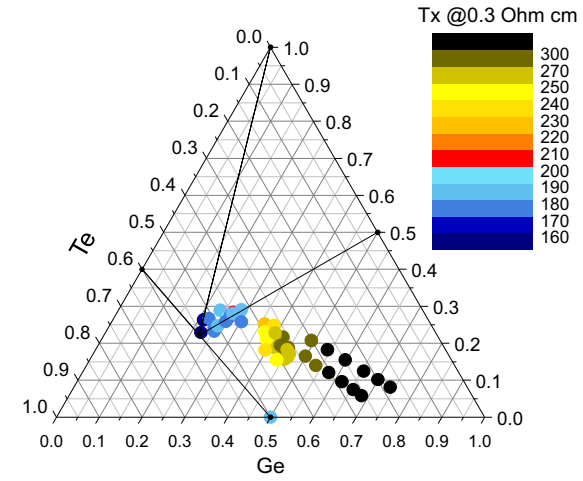

Fig. 2. Crystallization temperature as function of Ge–Sb–Te stoichiometry.

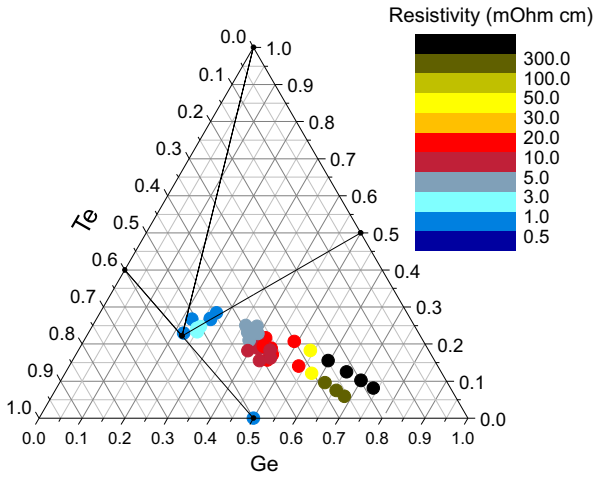

Fig. 3. Resistivity of the crystalline (SET) state as function of Ge–Sb–Te stoichiometry.

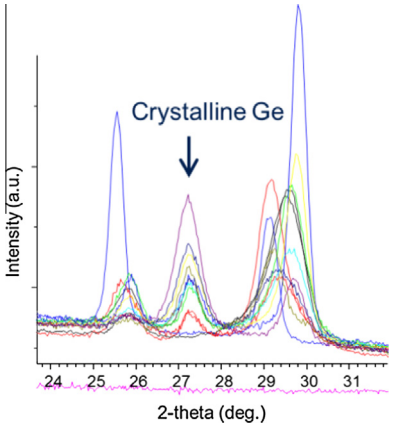

Fig. 4. Ge segregation detected on all the alloys explored above, after ~450 °C annealing. Ge segregation extent increasing with alloy Ge content.

4. Electrical characterization

A standard electrical characterization is performed on the PCM cells described in paragraph 2. Fig. 5 shows the *I–V* curves of amorphous state of D-alloy and T-alloy, compared with GST. The most