Solid-State Electronics 111 (2015) 47–51

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

An in-depth study of thermal effects in reset transitions in HfO_2 based RRAMs

M.A. Villena [a], M.B. González [b], J.B. Roldán [a,*], F. Campabadal [b], F. Jiménez-Molinos [a], F.M. Gómez-Campos [a], J. Suñé [c]

[a] Departamento de Electrónica y Tecnología de Computadores, Universidad de Granada, Facultad de Ciencias, Avd. Fuentenueva s/n, 18071 Granada, Spain
[b] Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain
[c] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Bellaterra, Cerdanyola del Vallès 08193, Spain

ARTICLE INFO

Article history:
Received 1 October 2014
Received in revised form 9 April 2015
Accepted 27 April 2015

Keywords:
RRAMs
Thermal effects
Device simulation
Quantum effects

ABSTRACT

Reset transitions in HfO_2 based RRAMs operated at different temperatures have been studied. Ni/HfO_2/Si-n^+ devices were fabricated and measured at temperatures ranging from 233 K to 473 K to characterize their reset features. In addition, a simulator including several coupled conductive filaments, series resistance and quantum effects was employed to analyze the same devices. The experimental results were correctly reproduced. It was found that the reset voltage and current show slight temperature dependence. To explain this fact, the roles of the out-diffusion of metallic species from the conductive filament and its conductance temperature dependence have been studied by simulation. The different conductive filament resistance components are also analyzed in the temperature range employed in our study. Finally, the thermal change in the energy barrier linked to quantum effects in the transport properties in the filament is modeled.

1. Introduction

Resistive Random Access Memories (RRAMs) are currently being studied by the scientific community to assess their potential to solve the limitations of flash technology in the non-volatile memory realm [1–3]. They have many interesting features such as a low program/erase current, fast speed, nano-scale operation characteristics, endurance, viability for 3D memory stacks and Complementary Metal Oxide Semiconductor (CMOS) technology compatibility [1,4].

RRAMs fabricated with metal oxides show different resistance states produced by alternating the formation and rupture of one or several conductive filaments (CFs) [3,5–8]: a low resistance state (LRS) is achieved if a CF is formed, and it can be switched to a high resistance state (HRS) by the partial dissolution of the CF (reset). The HRS can be turned back again to the LRS through a set process. An analysis (comparing experimental and simulation results) of the physics behind thermally assisted reset processes has been recently published in Refs. [9,10] for Cu/HfO_2/Pt devices and [11] for Ni/HfO_2/Si-n^+.

The analysis of these devices when operated at different temperatures is essential to understand the physical mechanisms involved in their switching behavior, since most of them are thermally assisted [12]. We deal with this issue in this work by comparing experimental and simulated results. In this respect, the different temperature dependencies found in RRAM charge conduction and CF rupture and creation processes are characterized by an in-depth simulation study. Both reset and set transitions have to be clearly known prior to solve the variability and endurance issues that remain a major barrier to massive industrial exploitation of RRAMs.

We have concentrated our analysis on reset processes. As explained in Ref. [11], the studied RRAM devices show nonlinear reset *I–V* curves at low applied voltages. Taking this nonlinearity into account, the charge transport along the CF can be explained by considering both the ohmic behavior in the wider part of the CF and quantum effects (we use the quantum point contact model [13] to account for them) in the narrow constrictions that show up in certain regions of the CF.

The experimental data we are using correspond to Ni/HfO_2/Si-n^+ devices fabricated at the IMB-CNM lab in Barcelona [14]. In these devices, the usual metal bottom electrode has been replaced by Si-n^+. This configuration is very interesting from the CMOS technology compatibility viewpoint since Ni has been

* Corresponding author.
E-mail address: jroldan@ugr.es (J.B. Roldán).

http://dx.doi.org/10.1016/j.sse.2015.04.008
0038-1101/

widely used in the main-stream CMOS technology as source/drain contact material and HfO_2 as the basic high-k insulator in MOS gate stacks from the 45 nm node onwards.

In the simulation ground we used a tool [9] that includes the possibility of several coupled CFs where conduction takes place (including quantum effects in the charge transport [11,15]). The current, temperature, and temporal evolution of each CF are calculated self-consistently. The series resistance at each CF (accounting for the Maxwell and the set-up resistances), the heat exchange with the electrodes and the oxide, and the resistance per unit length along each CF (dependent on the temperature and on the CF shape and width) have been taken into account.

The paper is organized as follows. In Section 2 we describe the fabricated devices and measurement set-up, Section 3 is devoted to the numerical simulator, and Section 4 to the discussion of the main results.

2. Device fabrication and measurement set-up

The Ni/HfO_2/Si-n^+ devices were fabricated on (100) n-type Czochralski silicon wafers with resistivity (7–13) mΩ cm. The process flow started with standard wafer cleaning followed by a wet thermal oxidation process at 1100 °C leading to a 400 nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Next, the 20 nm-thick HfO_2 layers were deposited by atomic layer deposition at 473 K using tetrakis (Dimethylamido)-hafnium (TDMAH) and H_2O as precursors, and N_2 as carrier and purge gas. Finally the top 200 nm-thick Ni electrode was deposited by magnetron sputtering, followed by a lift-off process. The area of the cells is $5 \times 5\ \mu m^2$, as defined by the field oxide patterning, i.e. metal contact pads lay on the field oxide.

The current–voltage (I–V) curves were measured using HP-4155B semiconductor parameter analyzer. The voltage was applied to the top Ni electrode, while the Si substrate was grounded. For this study, 500 successive cycles were measured at nine different temperatures (between 233 K and 473 K) by using an Espec ETC-200L thermal system. The set and reset currents were dynamically detected by connecting the I–V meter to the computer via GPIB (General Purpose Instrumentation Bus) and controlling it using MATLAB. See more details in [14].

3. Simulator description

The simulator characteristics are given in [9,11]. The RRAM simulator accounts for a structure with two different electrodes and an oxide, where the electrical and thermal properties of the materials are described. An arbitrary number of CFs with different radii and shapes can be considered, including the series resistance (calculated considering the set-up and Maxwell resistances of each CF). Taking into account the study of Ref. [16], where similar devices were used to those described in Section 2, truncated-cone-shaped CFs are employed with the narrowest end placed at the interface between the dielectric and the Si-n^+ layer.

The temporal evolution of the CFs is determined by calculating the diffusion processes of the metal atoms that form the CFs core. The temperature along the CFs is obtained solving the heat equation, where the heat dissipation to the electrodes and the surrounding oxide is considered. Once the resistance of the CFs is obtained, the device current is determined by considering all the CFs including their electrical coupling. In addition, quantum effects linked to the narrow CF constrictions located close to the Si-n^+ electrode contact region are accounted for. In our calculations, the temperature dependence of the conductivity and the CFs shape at each grid point between the electrodes are taken into consideration. The total electric current, temperature and time evolution of all the CFs are solved self-consistently. The set of constants employed to fit the measured curves can be found in Ref. [11].

Similar unipolar devices to ours were fabricated by other groups, Ref. [16]. These authors proved the presence of conductive filaments with a high concentration of Ni specie. According to Ref. [16,17], we assumed the CFs to be formed in a first stage by a percolation path of oxygen vacancies along which, in a second step, atoms from the metal electrode migrate in a movement linked to the high current density and high temperature produced in set processes. Taking into account these facts, we find reasonable considering reset transitions connected with thermal dissolution processes.

4. Results and discussion

We show in Fig. 1 an I–V curve for the devices described in Section 2. The experimental measurement (dashed lines) has been accurately reproduced with our simulator (solid lines) [11].

The curve shown in Fig. 1, where different current steps are seen, corresponds to a structure with several CFs (different RRAM configurations might show up several independent CFs or a main CF with several branches). This structure consists of a Ni/HfO_2/Si-n^+ device with four CFs with truncated-cone-shapes. The CFs have the following maximum radii (r_{CFmax}) and fraction of each r_{CFmax} in the narrowest part (C_{CFi}) [11]: $r_{CFmax} = 30$ nm and $C_{CF0} = 4.3\%$ for CF1, $r_{CFmax} = 3$ nm and $C_{CF0} = 4.3\%$ for CF2, $r_{CFmax} = 2.5$ nm and $C_{CF0} = 5\%$ for CF3, and $r_{CFmax} = 2$ nm, $C_{CF0} = 6\%$) for CF4. These CFs are electrically coupled, so their ruptures (the ruptures occur at different times, see the Supplementary Material included) produce partial reset processes characterized by current steps. The temperature of these CFs is increased by Joule heating until they get broken at the hottest region (in truncated-cone-shaped CFs this region is found at the narrowest part). Once the critical temperature is reached, the reset process is very fast due to self-acceleration effects [5,9].

The fabricated devices have undergone many switching cycles while the external temperature was changed. The experimental reset voltages, V_{RESET}, (Fig. 2a) and reset currents, I_{RESET}, (Fig. 2b)

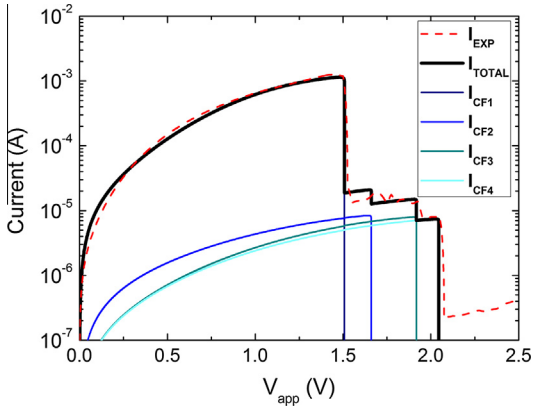

Fig. 1. RRAM current versus applied voltage. The experimental measurement of the devices described in Section 2 is shown in a dashed line and the simulation results are plotted in solid lines. The conductive path consists of four coupled truncated-cone-shaped CFs with the following sizes at the beginning of the simulation (r_{CFmax} accounts for the maximum radius of the CF and C_{CF0} is the fraction of this maximum radius in the narrowest part of the truncated cone). ($r_{CFmax} = 30$ nm, $C_{CF0} = 9\%$) for CF1, ($r_{CFmax} = 3$ nm, $C_{CF0} = 4.3\%$) for CF2, ($r_{CFmax} = 2.5$ nm, $C_{CF0} = 5\%$) for CF3 and ($r_{CFmax} = 2$ nm, $C_{CF0} = 6\%$) for CF4. The black line corresponds to the total current (I_{TOTAL}), while the other solid lines show the current for each filament (I_{CF1}, I_{CF2}, I_{CF3}, I_{CF4}). See more details on the simulations in the Supplementary Material.