Solid-State Electronics 111 (2015) 62–66

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors

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ARTICLE INFO

Article history:
Received 24 December 2014
Received in revised form 2 April 2015
Accepted 28 April 2015
Available online 25 May 2015

Keywords:
Tunnel field-effect transistor (FET)
Threshold voltage
Back bias

ABSTRACT

We investigated the impact of fin length (T_{fin}) on the threshold voltage (V_{th}) modulation by back bias (V_b) for independent double-gate (IDG) tunnel fin field-effect transistors (tFinFETs). It was found that V_{th} can be tuned by V_b for IDG tFinFETs regardless of T_{fin}, which can be explained by the back-gate-effect model of IDG FinFETs. For IDG tFinFETs, the slope (back-gate-effect factor (γ)) of V_{th} with respect to V_b increases with thinning T_{fin}. This means that T_{fin} thinning is effective for tuning V_{th} by V_b for IDG tFinFETs. Furthermore, it was demonstrated that this back-bias-effect is consistent with the results of device simulation using an advanced nonlocal band-to-band model.

1. Introduction

The increasing power consumption of complementary metal–oxide–silicon (CMOS) devices is a critical issue. To reduce the power consumption of CMOS devices, it is necessary to lower the operation voltage. To reduce the operation voltage, steeper subthreshold characteristic is one solution, which can be achieved by steep-slope device. Tunnel field-effect transistors (FETs) are candidate of steep-slope devices that have been reported to realize subthreshold slope (SS) of sub-60 mV/decade, which is smaller than the SS limitation for conventional metal–oxide–semiconductor FETs (MOSFETs) [1–10]. Since tunnel FETs (TFETs) are assumed to have ultralow voltage operation, the threshold voltage (V_{th}) control and design requirements for TFETs are severe compared with those for MOSFETs.

V_{th} tuning by back bias (V_b) is a promising method of V_{th} control for TFETs. It has been reported that V_{th} can be modulated by V_b for planar silicon-on-insulator (SOI) TFETs [11]. Thinning of buried oxide between the channel and the back gate is effective for lowering V_b of SOI TFETs [11]. In the case of independent double-gate (IDG) structure [12–14], since the dielectric between the channel and the back gate corresponds to the gate dielectric, this buried dielectric can be thinned to the gate dielectric thickness. V_b can be lowered to the operation voltage region by using the IDG structure. However, the influence of channel thickness on the V_{th} modulation by V_b for TFETs has not been clearly understood yet.

In this work, we studied the mechanism of the V_{th} modulation by V_b for IDG tFinFETs using our developed simulation [15,16]. We investigated the impact of fin length on the V_{th} modulation by V_b for IDG tunnel FinFETs (tFinFETs).

2. Experiment

We fabricated p-type IDG tFinFETs. (110) fin channel was formed on (100) SOI substrate. n^+poly-Si/$HfAlO_x$/SiO_2 (equivalent oxide thickness (EOT) = 1.5 nm) gate stacks were formed, patterned, and etched. The channel length was 230 nm. As ions with doses of 1.0×10^{15} cm^{-2} were implanted at 5 keV in the source region, while BF_2 ions with doses of 1.0×10^{15} cm^{-2} were implanted at 5 keV in the drain region [4]. The sidewalls were fabricated. Subsequently, to independently control the gates, the gate separation process was performed [12–14]. Next, to suppress the spread of the implanted dopant by activation annealing, we carried out flash lamp annealing (1200 °C, 3 ms) [17]. After Al electrode metallization, forming gas annealing was performed at 450 °C in an atmosphere of 97% N_2 + 3% H_2.

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http://dx.doi.org/10.1016/j.sse.2015.04.011
0038-1101/

In this study, V_{th} was defined as the gate voltage (V_g) at the drain current (I_d) = -10^{-12} A/μm, which corresponds to the minimum SS.

3. Results and discussion

Fig. 1 shows a cross-sectional transmission electron microscopy (TEM) image of the fabricated IDG tFinFETs. The fin length was defined as the length of the fin bottom. Since the n$^+$poly-Si gate is separated on the fin, the first gate (G1) and second gate (G2) can be independently controlled. In this case, G1 is the drive gate and G2 is the V_{th} control gate.

Fig. 2 shows I_d–V_d characteristics for tFinFETs in the double gate mode. Sub linear I_d (lower V_d) and I_d saturation which are typical of the Zener tunneling process. The saturation current like FETs is shown in tFinFETs. Leonelli et al. have reported that the performance of TFETs is improved by using a double gate because of the improvement of electrical-static control [8].

Fig. 3 shows the $|I_d|$–first-gate voltage (V_{g1}) characteristics for different back biases of p-type IDG tFinFETs with T_{fin} = 20 nm. V_b is V_{g2}–$V_{th(DG)}$, where V_{g2} is the second-gate voltage and $V_{th(DG)}$ is V_{th} for double-gate (DG)-mode tFinFETs. The on current for IDG tFinFETs increases with increasing back bias. Applying the back bias improves the electrostatic control on the gate 1 side. Since the gate electrodes of gate 1 and gate 2 are the same, the exchange of gate 1 and gate 2 has no impact on the TFET characteristics. The $|I_d|$–V_{g1} curves parallel shift for V_b = −0.1–1.4 V, and also V_{th} shifts

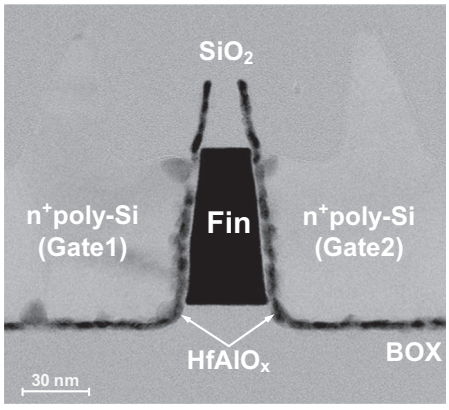

Fig. 1. Cross-sectional TEM image of fabricated IDG tFinFETs. The n$^+$poly-Si film is separated by the gate separation process. Each gate can be independently controlled.

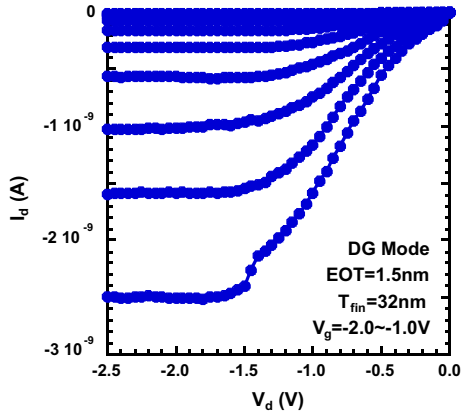

Fig. 2. I_d–V_d characteristics for tFinFETs with T_{fin} = 32 nm in the double gate mode.

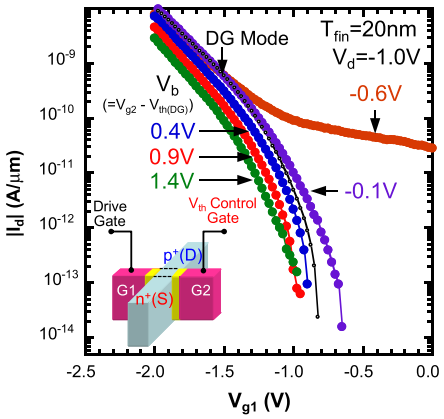

Fig. 3. $|I_d|$–V_{g1} characteristics for different back biases (V_b) of p-type IDG tFinFETs with T_{fin} = 20 nm. The channel length is 230 nm. The inset is a schematic illustration of IDG tFinFETs. G1 is the drive gate and G2 is the V_{th} control gate. The $|I_d|$–V_{g1} curves are parallel-shifted by V_b. SS slightly changes by V_b. However, in the case of the V_{th} shift in the positive direction, $|I_d|$ dramatically increases in the OFF region because the channel on the G2 side is in the ON state.

in the negative direction with increasing V_b. Thus, V_{th} for IDG tFinFETs can be modulated by V_b. In the case of V_b = −0.6 V, $|I_d|$ dramatically increases in the OFF region because the TFET on the G2 side is in the ON state. The suppression method of this dramatically increased $|I_d|$ is discussed in the final paragraph before the conclusion. (We confirmed by simulation as follows. The characteristics are the same for n-type and p-type TFETs and that V_{th} for n-type IDG tFinFETs is modulated by V_b. When a positive bias V_b is applied for n-type TFETs, the ambipolarity is observed.)

Fig. 4 shows the $|I_d|$–V_{g1} characteristics for V_b = 0.4 and 0.9 V of p-type IDG tFinFETs with T_{fin} = 20 nm. The device structure of the simulation is set to be the same as the fabricated device structures (Fig. 5(a)). The dopant profiles in the n$^+$, p$^-$, and p$^+$ layers are assumed to a constant profile. The dopant concentration in the n$^+$ layer is 1.0×10^{20} cm^{-3}, that in the p$^-$ layer is 2.0×10^{15} cm^{-3}, and that in the p$^+$ layer is 1.0×10^{20} cm^{-3}. The band-to-band tunneling rate was calculated using a nonlocal model [15,16]. The value of the A and B factors in Kane's parameters were taken from Ref. [18]. As shown in Fig. 4, the measured data for V_b = 0.4 and 0.9 V are well fitted to the simulation results. This means that our developed simulation can precisely estimate the TFET characteristics for V_b.

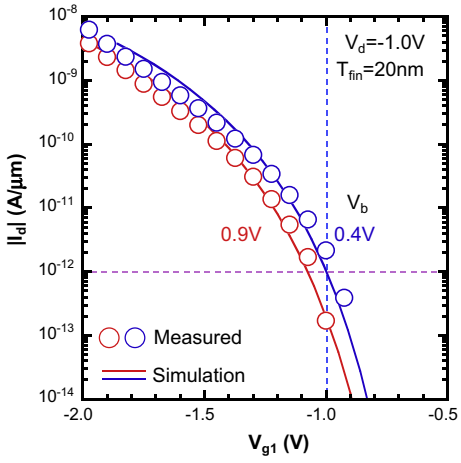

Fig. 4. $|I_d|$–V_{g1} characteristics of p-type IDG t-FinFETs for V_b = 0.4 and 0.9 V. Measured data for V_b = 0.4 and 0.9 V are well fitted to the simulation results.