Solid-State Electronics 111 (2015) 123–128

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction

T.A. Karatsori [a,b,*], C.G. Theodorou [a], E.G. Ioannidis [a], S. Haendler [c], E. Josse [c], C.A. Dimitriadis [b], G. Ghibaudo [a]

[a] IMEP-LAHC, INPG – Minatec, 3 Parvis Louis Néel, CS 50257, 38016 Grenoble, France
[b] Department of Physics, Aristotle University of Thessaloniki, Thessaloniki 54124, Greece
[c] STMicroelectronics, BP16, 38921 Crolles, France

ARTICLE INFO

Article history:
Received 16 January 2015
Received in revised form 24 April 2015
Accepted 1 June 2015
Available online 14 June 2015

Keywords:
Electrical parameter extraction
MOSFET
FDSOI

ABSTRACT

A new full gate voltage range methodology using a Lambert *W* function based inversion charge model, for extracting the electrical parameters in FDSOI nano-MOSFET devices, has been developed. Split capacitance–voltage measurements carried out on 14 nm technology FDSOI devices show that the inversion charge variation with gate voltage can be well described by a Lambert *W* function. Based on the drain current equation in the linear region including the inversion charge described by the Lambert function of gate voltage and the standard mobility equation enables five electrical MOSFET parameters to be extracted from experimental I_d–V_g measurements (ideality factor, threshold voltage, low field mobility, first and second order mobility attenuation factors). The extracted parameters were compared with those extracted by the well-known Y-function in strong inversion region. The present methodology for extracting the electrical MOSFET parameters was verified over a wide range of channel lengths on nano-scale FDSOI devices, demonstrating its simplicity, accuracy and robustness.

1. Introduction

The accurate determination of the MOSFET electrical parameters is essential for understanding the physics and engineering of the devices, particularly for advanced ultra-scaled devices. A lot of methods have been proposed for the MOSFET parameter extraction but they are generally restricted to the above threshold region and mostly assume that the inversion charge varies linearly with gate voltage overdrive [1–11]. As the supply voltage Vdd is reduced with device scaling, the operating gate bias moves closer to the threshold voltage (near threshold operation), and the assumption that the inversion charge varies approximately linearly with gate voltage overdrive becomes less and less accurate. Few attempts to extend the parameter extraction from above to near threshold region was carried out using $g_m/I_d(V_g)$ derivative [12], Lambert *W* function [13] or logarithmic function [14] of gate voltage overdrive for the inversion charge control, but it was not applied to the entire gate voltage range from weak to strong inversion.

The goal of this paper is to present a new methodology based on the Lambert *W* (LW) function, which allows the extraction of MOSFET parameters over the full gate voltage range i.e. from weak to strong inversion region, enabling to fully capture the transition between subthreshold and above threshold region, despite the reduction of supply voltage. To this end, we first validate the usefulness of the LW function to describe accurately the gate-to-channel capacitance characteristics $C_{gc}(V_g)$, and, by turn, the MOSFET inversion charge $Q_i(V_g)$ from weak to strong inversion region. Then, in conjunction with the conventional mobility expression, we apply this analytical $Q_i(V_g)$ law for the parameter extraction in advanced MOS devices from a 14 nm FDSOI CMOS technology.

2. Experimental details

Electrical measurements were performed on both n-MOS and p-MOS transistors issued from an advanced FD-SOI CMOS technology [15]. They were fabricated on (100) SOI wafers with 20 nm thin BOX and a Si (SiGe for p-MOS) body thinned down to 6 nm. The mid-gap metal gate/high k dielectric front gate stack features a 1.2 nm equivalent oxide thickness (EOT) and 1.5 nm for n-MOS and p-MOS respectively. The Si or SiGe channels are left undoped. The channel length (L) is varying from 3 down to 0.018 μm and the channel width (W) is fixed at 10 μm. Both gate-to-channel capacitance and drain current measurements were performed at zero

* Corresponding author at: IMEP-LAHC, INPG – Minatec, 3 Parvis Louis Néel, CS 50257, 38016 Grenoble, France.

http://dx.doi.org/10.1016/j.sse.2015.06.002
0038-1101/

back gate bias voltage using the Agilent B1500/1530 Semiconductor Device Analyzer.

3. Parameter extraction methodology

The proposed parameter extraction methodology was developed with the following steps. First, typical $C_{gc}(V_g)$ characteristics were obtained on large area 14 nm FDSOI MOS devices. Note that $C_{gc}(V_g)$ measurements were not carried out on smaller area single devices for accuracy reason, since no specific test structure was available in our test mask with many devices in parallel for permitting such measurements on small gate lengths. These data were used to calculate the corresponding inversion charge $Q_i(V_g)$ and to fit the gate-to-channel capacitance with a theoretical expression, and extract the gate oxide capacitance per unit area C_{ox} and the subthreshold ideality factor n. Then, the inversion charge data were fitted with the LW function based model using three parameters, i.e. C_{ox}, n and the threshold voltage V_t, validating the adequacy of the LW function for describing the inversion charge from weak to strong inversion in a continuous way.

In a second step, the drain current $I_d(V_g)$ data obtained in linear region on varying channel length devices were fitted using the LW based $Q_i(V_g)$ expression and the standard three parameter mobility model, including the low field mobility μ_0 and the first order θ_1 and second order θ_2 attenuation coefficients [13,16].

3.1. Lambert W function based inversion charge control law with gate voltage

The Lambert W function has been shown to be very efficient for describing $C_{gc}(V_g)$ characteristics in FDSOI devices [17]. Here, we further verify that it is still applicable to 14 nm FDSOI devices. Indeed, considering the charge conservation equation in FDSOI devices and the fact that in standard FDSOI the relation $C_{box} \ll C_{ox}$ is valid, where C_{box} is the BOX oxide capacitance the front gate-to-channel capacitance can be described by:

$$C_{gc}(V_g) = \frac{\beta Q_i(V_g) C_{ox}}{C_{ox} + \beta Q_i(V_g)} \tag{1}$$

where $\beta = q/(nkT)$, n is the ideality factor, q is the electron charge and kT is the thermal energy.

Fig. 1 shows that Eq. (1) provides a very good description of $C_{gc}(V_g)$ for 14 nm FDSOI devices both in linear and logarithmic scales using C_{ox} and n in Eq. (1) as fitting parameters. As is usual in split C–V technique, the inversion charge can be deduced by integration of $C_{gc}(V_g)$ curve between $V_g = 0$ and V_g. It should be noted that the calculated maximum fitting error does not exceed ≈10% over the whole gate voltage range, which is really good given the large C_{gc} dynamic investigated (≈3 decades).

Therefore, the experimental $Q_i(V_g)$ characteristics can be reproduced using the Lambert W function of gate voltage for the inversion charge Q_i in terms of the gate oxide capacitance per unit area C_{ox}, the subthreshold ideality factor n and the threshold voltage V_t [17]:

$$Q_i(V_g) = C_{ox} n \frac{kT}{q} \mathrm{LW}\left(e^{q\frac{V_g - V_t}{nkT}}\right). \tag{2}$$

Fig. 2 shows that the LW function in Eq. (2) enables a very good fitting of the inversion charge from weak to strong inversion using the three parameters C_{ox}, n and V_t. In this example, a Levenberg–Marquardt non linear regression has been used to extract the best fitting parameters: $C_{ox} = 2.6 \times 10^{-6}$ F/cm^2, $n = 1.37$ and $V_t = 0.30$ V in n-MOS devices and $C_{ox} = 1.44 \times 10^{-6}$ F/cm^2, $n = 1.53$ and $V_t = 0.34$ V in p-MOS devices. It should be mentioned that the extracted values of C_{ox} and n were consistent with those used for the $C_{gc}(V_g)$ fitting (see Fig. 1) and the calculated maximum fitting error is no more than ≈11% for n-MOS and ≈25% for p-MOS for the *whole* V_g range. This finding demonstrates that the LW function in Eq. (2) constitutes an accurate, continuous and analytical expression for the MOSFET inversion charge with gate voltage applicable from weak to strong inversion both in linear and logarithmic scale.

3.2. MOSFET parameter extraction procedure from drain current characteristics

The drain current of a MOSFET in linear operation reads:

$$I_d = \frac{W}{L} \mu_{eff} Q_i V_d \tag{3}$$

where μ_{eff} is the effective mobility and V_d is the drain voltage. From the conventional formulation of the effective mobility in strong inversion, i.e. with gate voltage drive [16], μ_{eff} can be expressed with the inversion charge as:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 \frac{Q_i}{C_{ox}} + \theta_2 \left(\frac{Q_i}{C_{ox}}\right)^2}, \tag{4}$$

where μ_0 is the low field mobility and θ_1, θ_2 are the first and second order mobility attenuation factors, respectively. Note that $\theta_1 = \theta_{10} + R_{sd} \cdot G_m$, with $G_m = (W/L) \cdot \mu_0 \cdot C_{ox}$ and R_{sd} being the source–drain series resistance [2].

Since the LW function based inversion charge expression of Eq. (2) is well appropriate from weak to strong inversion region, it can be used in Eqs. (3), (4) for a full gate voltage range MOSFET parameter extraction with overall 5 parameters, i.e. V_t, n, μ_0, θ_1 and θ_2. We

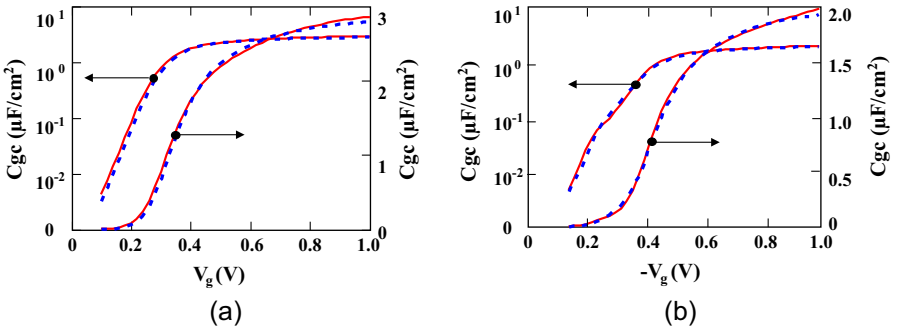

Fig. 1. Experimental (solid lines) and modeled (dashed lines) $C_{gc}(V_g)$ characteristics of n- and p-channel FD-SOI MOSFETs with channel width $W = 10$ μm and channel length $L = 3$ μm. The modeled results were obtained using the parameters: $C_{ox} = 2.6 \times 10^{-6}$ F/cm^2 and $n = 1.37$ for the n-MOS device (a) and $C_{ox} = 1.44 \times 10^{-6}$ F/cm^2 and $n = 1.53$ for the p-MOS device (b).