



Experimental study of electron mobility characterization in direct contact La-silicate/Si structure based nMOSFETs

T. Kawanago^{a,*}, Y. Lee^a, K. Kakushima^b, P. Ahmet^a, K. Tsutsui^b, A. Nishiyama^b, N. Sugii^b, K. Natori^a, T. Hattori^a, H. Iwai^a

^a Frontier Research Center, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan

^b Interdisciplinary Graduate School of Science, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan

ARTICLE INFO

Article history:

Available online 18 May 2012

Keywords:

Direct-contact high-*k*/Si structure
Rare earth oxides
Silicate
EOT
Effective mobility

ABSTRACT

This study focuses on studying the effective electron mobility in direct contact La-silicate/Si structure based nMOSFETs and searching for the difference of the mobility characteristics compared with the SiO₂ MOSFETs. In this study, three types of gate electrode structure were prepared to investigate the mobility characteristics over a wide EOT range; W for EOT of 1.63 nm, TiN/W for EOT of 1.02 nm and metal-inserted poly-Si (MIPS) for EOT of 0.71 nm. Since the silicate formation is basically caused by the presence of oxygen, Si layer in MIPS can suppress the oxygen in-diffusion from atmosphere, resulting in scaled EOT. It is found that the E_{eff} dependence of mobility with La-silicate is observed to differ from the mobility of SiO₂ MOSFETs. The electron mobility with La-silicate shows the weaker E_{eff} dependence than the mobility of SiO₂ nMOSFETs in middle and high E_{eff} region. This suggests an existence of additional mobility component related to the direct contact La-silicate/Si structure. The effective electron mobility is degraded with decreasing EOT in entire E_{eff} region. This means that the scattering sources including Coulomb scattering, phonon scattering and surface roughness scattering are located not at La-silicate/Si interface but the inside of gate stacks and approach the Si inversion channel. Coulomb scattering and phonon scattering are thought to be strengthened by increasing *k*-value because of the enhancement of Coulomb scattering potential and higher ionicity in La-silicate gate dielectrics. The influence of metal/high-*k* interface is also considered to affect on the mobility with decreasing the EOT.

© 2012 Elsevier Ltd. All rights reserved.

1. Introduction

Reduced carrier mobility is one of the crucial problems in high-*k*/metal gate stack MOSFETs [1]. Several scattering mechanisms inherent to high-*k* gate dielectrics has been proposed to understand the physical origins of the mobility degradation, such as remote Coulomb scattering (RCS) caused by fixed charges inside high-*k* gate dielectrics, remote phonon scattering (RPS) originating from low-energy optical phonon modes in high-*k* gate dielectrics and remote surface roughness scattering (SRS) [1,2]. The carrier mobility can be recovered by insertion of SiO₂ interfacial layer (IL) because scattering sources separate from inversion channel [1]. However, removal of the IL is essential issue for reduction of equivalent oxide thickness (EOT) in high-*k*/metal gate stacks. Continued scaling in the EOT highly contributes to suppress the short-channel effect and threshold voltage variability in advanced MOSFETs [3,4]. In particular, small threshold voltage variability is required for decreasing power supply voltage, resulting in low

power consumption. Therefore, the direct contact of high-*k*/Si structure is strongly needed.

The direct contact high-*k*/Si structure has been reported with Hf-based oxides to scavenge the IL by sophisticated method [5]. Moreover, the direct contact high-*k*/Si structure can be realized by using La₂O₃ as gate dielectrics because of a form La-silicate by the silicate reaction between La₂O₃ and Si at interface [6]. Advantage of this method is that the direct contact high-*k*/Si structure can be easily achieved by simply depositing the La₂O₃ on Si substrate. The scaled EOT and superior interfacial property has been demonstrated in direct contact La-silicate/Si structure by metal-inserted poly-Si (MIPS) in conjunction with high temperature annealing [6].

Multiple studies regarding Hf-based oxides have revealed that the carrier mobility is decreased with decreasing the IL thickness [7]. Most of the published works were carried out on the presence of SiO₂ IL in high-*k*/metal gate stacks. It is thus of great importance to study the carrier mobility in MOSFETs with direct contact high-*k*/Si structure for determining the performance of highly scaled MOSFETs. The objective in this study is to obtain the better understanding of carrier mobility in direct contact La-silicate/Si structure

* Corresponding author. Tel.: +81 45 924 5847; fax: +81 45 924 5846.

E-mail address: kawanago.ta@n.titech.ac.jp (T. Kawanago).

based nMOSFETs with a wide range of EOT. The impact of IL-free structure on carrier mobility is experimentally investigated. The physical origin is also discussed based on the experimental results.

2. Device fabrication

La_2O_3 in 3 nm thickness was deposited on HF-last p-Si substrate by e-beam evaporation in an ultra-high vacuum chamber, followed by *in situ* W (tungsten) metal deposition by RF sputtering. TiN and Si were deposited on W metal for MIPS stacks. The physical thickness of W, TiN and Si were 5 nm, 10 nm and 100 nm, respectively. Source and drain pre-formed p-Si (100) substrates were utilized to fabricate nMOSFETs. The substrate impurity concentration of MOSFETs is $3 \times 10^{16} \text{ cm}^{-3}$. The thermally-grown SiO_2 nMOSFETs was also fabricated with same substrate impurity concentration. The metal was patterned by reactive ion etching (RIE) with SF_6 chemistry to form gate electrodes. The samples were post-metallization annealed in forming gas ambient ($\text{H}_2:\text{N}_2 = 3\%:97\%$) at 800°C for 30 min to form the La-silicate by the reaction with Si substrate [6]. Al was deposited on the source/drain region and back side of the substrate as a contact. Finally, recovery annealing (FGA) was performed. Process flow and fabricated device structures are summarized in Fig 1a and b. EOT was estimated by NCSU CVC program [8]. Split-CV method was employed to measure an effective mobility of nMOSFETs [9].

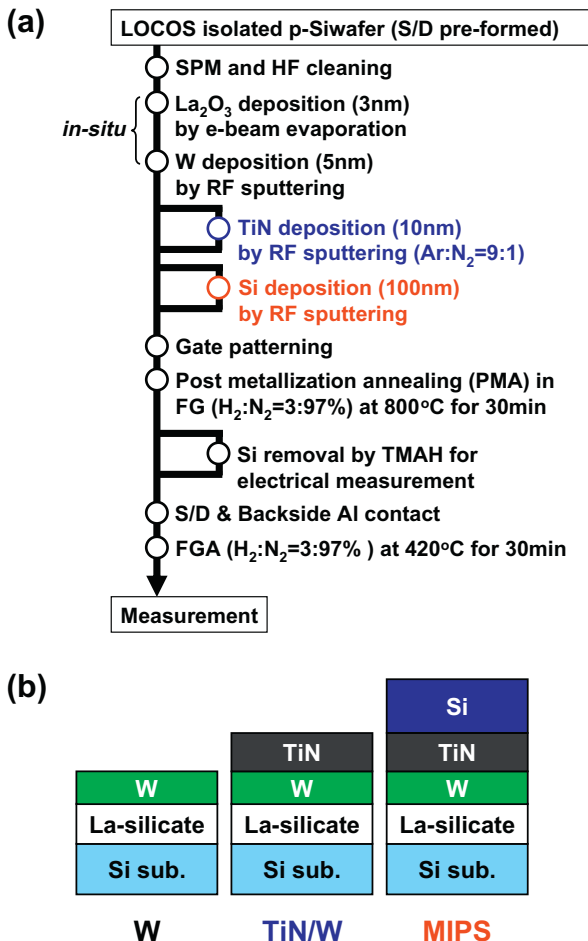


Fig. 1. (a) Process flow of nMOSFETs and (b) fabricated device structures, respectively.

3. Results and discussion

The details of fabricated MOSFETs in this study are summarized in Table 1. It is worth pointing out that these three devices were fabricated at the same time. This means that the physical thickness of La_2O_3 and W metal are completely same in these three types of MOSFETs. An average k -value in overall gate dielectrics was estimated from EOT and cross-sectional TEM observations. Using the W metal yields the EOT of 1.63 nm, while the EOT of 0.71 nm can be obtained by MIPS stacks. The formation of La-silicate is attributed to the Si diffusion from substrate to La_2O_3 , and hence it results in not a bilayer structure of La-silicate/ La_2O_3 but a compositional gradient in La-silicate dielectrics by annealing at 800°C for 30 min in forming gas ambient [10]. The k -value of La-silicate is decreased with increasing Si content in gate dielectrics similar to HfSiON [11,12]. The formation of La-rich silicate by suppressing excess silicate reaction is key issue for achieving scaled EOT. Since the silicate reaction is basically triggered by the existence of oxygen during annealing process, Si layer in MIPS stacks can prevent the oxygen diffusion from atmosphere during annealing process, resulting in the suppression of excess silicate reaction [6]. The threshold voltage (V_{th}) and sub-threshold slope (SS) are almost identical regardless of gate stacks. This strongly suggests that the significant interface traps are not generated and superior interfacial property is maintained even at EOT of 0.71 nm. Fig. 2 shows the gate leakage current (J_g) at gate voltage (V_g) of 1 V as a function of EOT. The gate leakage current is increased with decreasing EOT. According to the previous study, band gap of La_2O_3 is 5.5 eV, while the band gap of La-silicate is increased up to about 6 eV [11]. It should be noted that the band gap of high- k dielectrics is inversely proportional to the dielectrics constant [11]. As a result, the band gap of Si-rich silicate is larger than that of La-rich silicate [11]. In addition, contrast change in the gate dielectrics adjacent to Si substrate and increasing physical thickness of the overall gate dielectrics were observed from cross-sectional TEM images when W single layer was utilized as gate electrode, indicating the formation of Si-rich silicate. On the other hand, contrast change cannot be observed in the case of MIPS structure. Therefore, increasing gate leakage current with decreasing EOT is likely caused by suppressing excess silicate reaction and the formation of La-rich silicate with smaller band gap. Fig. 3 shows the effective electron mobility as a function of EOT at measurement temperature of 300 K. The effective electron mobility is monotonically decreased with decreasing EOT in the entire effective field (E_{eff}). It is well known that the inversion layer mobility in Si MOSFETs can be divided into three scattering mechanisms, namely Coulomb scattering, phonon scattering and surface roughness scattering [13]. From Fig. 3, effective electron mobility is found to be limited by all of three components with decreasing EOT. The E_{eff} dependence of mobility for La-silicate is weaker than that for SiO_2 in middle E_{eff} region, indicating the influence of the remote phonon attributed to La-silicate gate dielectrics [2]. Furthermore, at high E_{eff} , mobility of La-silicate shows gradual E_{eff} dependence compared with that of SiO_2 and surpasses the mobility of SiO_2 at E_{eff} higher than 1 MV/cm. The different characteristics for the mobility are clearly observed as shown in Fig. 3. However, reducing mobility with decreasing the EOT is similar to the Hf-based oxides [7]. Previous study has reported that

Table 1
Details of fabricated MOSFETs in this study.

Gate structure	k -value	EOT (nm)	V_{th} (V)	SS (mV/dec)
W	8	1.63	−0.06	65
TiN/W	12	1.02	−0.12	66
MIPS	16	0.71	−0.14	67

Download English Version:

<https://daneshyari.com/en/article/7151081>

Download Persian Version:

<https://daneshyari.com/article/7151081>

[Daneshyari.com](https://daneshyari.com)