Solid-State Electronics 74 (2012) 19–24

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

On the efficiency of stress techniques in gate-last n-type bulk FinFETs

Geert Eneman [a,*], Nadine Collaert [a], Anabela Veloso [a], An De Keersgieter [a], Kristin De Meyer [a,b], Thomas Y. Hoffmann [a,1], Naoto Horiguchi [a], Aaron Thean [a]

[a] Imec, Kapeldreef 75, 3001 Heverlee, Belgium
[b] ESAT-INSYS, K.U. Leuven, Belgium

ARTICLE INFO

Article history:
Available online 28 April 2012

Keywords:
FinFET
n-Type MOSFET
Strain
Stress
TCAD
Replacement gate

ABSTRACT

This paper presents a TCAD study on the effectiveness of stress techniques on bulk FinFETs and planar nFETs, comparing gate-first and gate-last schemes.

It is shown that strained Contact Etch-Stop Layers (CESLs) are about 30–40% less effective in narrow FinFETs than on planar FETs when a gate-first scheme is used. On the other hand, using a gate-last scheme significantly enhances CESL effectiveness both on FinFETs and planar FETs, especially when the device width is scaled.

A tensile gate fill material leads to a completely different channel stress configuration in gate-last than in gate-first nFETs. While for gate-first FinFETs, this leads to up to 10% mobility improvement at narrow widths, mobility degradation is predicted when tensile gates are used in a gate-last configuration. For this stressor, FinFETs show a different width dependence than planar FETs due to perpendicular stress in the fin sidewall, leading overall to higher mobilities in FinFETs than in their planar counterparts.

1. Introduction

Gate-last processes are adopted nowadays for high-performance CMOS applications, as it facilitates using high-κ dielectrics and metal gates, moreover it has been indicated that the efficiency of several stress techniques is enhanced after gate removal [1]. On the other hand, bulk FinFETs are considered for future technology nodes thanks to their improved electrostatics and scalability [2]. For conventional gate-first schemes, there have been several reports on the compatibility of the FinFET architecture with stress techniques, such as strained Contact Etch-Stop Layers (CESLs) and $Si_{1-x}Ge_x$ source/drain stressors [3–5].

When considering the commercial viability of combining gate-last schemes with FinFET architectures, the compatibility with stress techniques is of crucial importance. However, to our knowledge there have been little or no reports on this. This TCAD work focuses on the efficiency of two stress techniques, tensile CESL and a tensile tungsten gate fill, when used in combination with short-channel isolated bulk n-type FinFETs, either with a gate-first or gate-last scheme.

2. Setup

2.1. Simulation overview

All simulations are performed for transistors oriented in the ⟨011⟩ direction on (100) wafers using Sentaurus-Process, a commercially available CMOS process simulator [6]. Fig. 1 details the simulation steps used for the gate-last and gate-first processing schemes. Table 1 shows the default dimensions used and indicates that the devices under study here are single-fin, isolated (i.e. large fin and poly pitch), short-channel fin structures. The transistor width is the main parameter that is varied, between 500 and 10 nm.

A typical fin structure with a gate-last scheme is shown in Fig. 2. Dirichlet boundary conditions were used at the simulation boundaries, i.e. zero velocities in the direction perpendicular to the boundary plane, while free-standing surfaces have zero normal stress. For these conditions, simulations of quarter-FinFETs are sufficient. Fig. 2 shows the main stress directions: the longitudinal (zz) component σ_{zz} runs from source to drain, the vertical (xx) component σ_{xx} is perpendicular to the wafer surface, and the perpendicular (yy) component σ_{yy} runs across the width of the transistor. Tensile stresses are positive, compressive stresses have negative value.

An intrinsic stress σ_0 in three dimensions is specified into the CESL or tungsten stressor. After deposition on a planar Si wafer, this would lead to a resulting two-dimensional stress σ_{2D} given by:

* Corresponding author.
E-mail address: geert.eneman@imec.be (G. Eneman).
[1] Present address: SuVolta, Inc., Los Gatos, CA, USA.

0038-1101/$ - see front matter © 2012 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.sse.2012.04.006

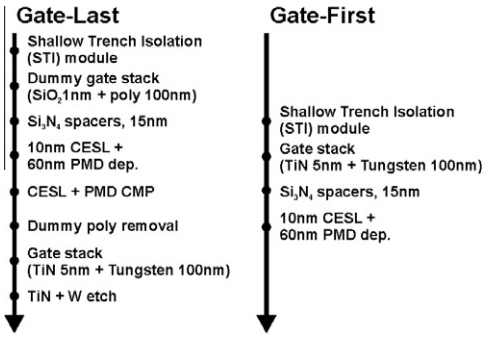

Fig. 1. Simulation steps for gate-last (left) and gate-first (right) simulations. PMD = Pre-metal dielectric.

Table 1
Overview of fin dimensions used in this work. Other dimensions and thicknesses are specified in Fig. 1.

FinFET type	Bulk FinFETs
Fin height (F_H)	35 nm or 0 nm (i.e. planar)
Fin width (W)	500 → 10 nm
Gate length (L_G)	20 nm
Spacer width	15 nm
Poly pitch	500 nm
Fin pitch	Fin width + 200 nm

$$\sigma_{2D} = \sigma_0 \cdot \frac{1-2\nu}{1-\nu} \tag{1}$$

ν is the Poisson's ratio of the stressor (0.3 for CESL/Si_3N_4, 0.296 for tungsten). σ_{2D} is the value that is typically extracted from wafer bending experiments.

2.2. Calculating mobility enhancement

This work will attempt to give a first-order, qualitative estimate of the mobility enhancement that can be expected for a particular fin dimension. In order to do this, the three stress components σ_{xx}, σ_{yy} and σ_{zz} are extracted along cutlines, 2 nm below the surface of the top of the fin, or 2 nm beside the fin sidewall (top and side cutlines, Fig. 2). These components are averaged along the length of the channel:

$$\sigma_{ii,av} = \frac{2}{L_G}\int_{L_G/2} \sigma_{ii} \cdot dz \text{ for ii} = xx, yy, zz \tag{2}$$

L_G is the channel length. For each cutline, the average stress components $\sigma_{ii,av}$ are then combined into $\vec{\sigma}_{av,top,side}$ to calculate the change in mobility using standard piezoconductance:

$$\partial\mu_{top,side} = \vec{\Pi} \cdot \vec{\sigma}_{av,top,side} \tag{3}$$

$\vec{\Pi}$ is a piezoconductance tensor for $\langle 011\rangle/(100)$ nFET channels, using the values reported by Smith for electrons in silicon [7]. Depending on the top or the side of the fin, the absolute mobility is estimated as:

$$\mu_{top}(y) = \mu_{0,top} \cdot [1 + \partial\mu_{top}(y)] \tag{4}$$

$$\mu_{side}(x) = \mu_{0,side} \cdot [1 + \partial\mu_{side}(x)] \tag{5}$$

For the unstrained mobilities $\mu_{0,top}$ and $\mu_{0,\,side}$, values of 240 and 90 cm^2/Vs are used, respectively, based on literature values for electron mobilities of the appropriate surface orientations at an inversion sheet density of 1×10^{13} cm^{-2} [8].

The total average mobility is obtained through integration along the top and the sides of the fin:

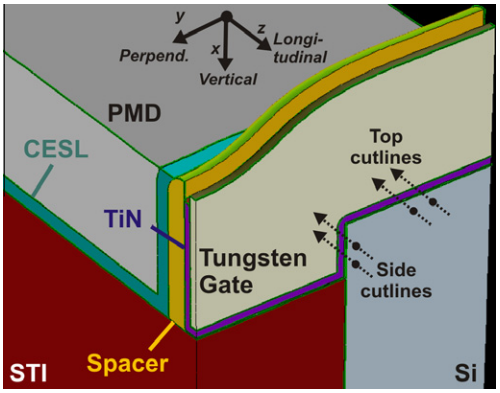

Fig. 2. Cross-section of a 200 nm-wide fin with a gate-last module.

$$\mu_{total} = \frac{\int_{top}\mu_{top}(y)\cdot dy + 2\cdot\int_{side}\mu_{side}(x)\cdot dx}{W + 2\cdot F_H} \tag{6}$$

W and F_H are the fin width and height, respectively. The final total mobility improvement for this fin width and height is then given by:

$$\partial\mu_{total} = \frac{\mu_{total} - \mu_{0,total}}{\mu_{0,total}} \tag{7}$$

where $\mu_{0,total}$ is the averaged unstrained mobility:

$$\mu_{0,total} = \frac{\mu_{0,top}\cdot W + 2\cdot\mu_{0,side}\cdot F_H}{W + 2\cdot F_H} \tag{8}$$

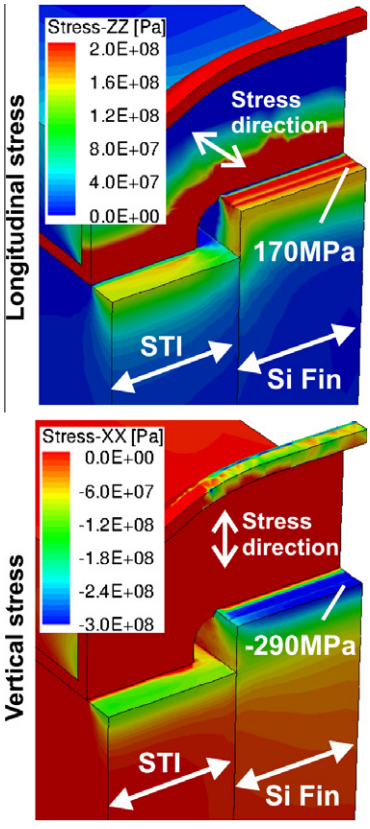

Fig. 3. Stress contours in a 200 nm-wide FinFET with a gate-first scheme, for the case of a 10 nm-thick CESL with +2 GPa intrinsic tensile stress. The gate and spacer regions have been omitted from this view. (Top) Longitudinal stress. (Bottom) Vertical stress.