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Understanding device performance by incorporating 2D-carrier profiles from high resolution scanning spreading resistance microscopy into device simulations

Aftab Nazir [a,b,*], Pierre Eyben [a], Trudo Clarysse [a], Geert Hellings [a,c], Andreas Schulze [a,b], Jay Mody [a,b], Kristin De Meyer [a,b], Hugo Bender [a], Wilfried Vandervorst [a,b]

[a] Imec, Kapeldreef 75, B-3001 Leuven, Belgium
[b] Department of Physics and Astronomy, KU Leuven, Leuven, Belgium
[c] Department of Electrical Engineering, KU Leuven, Leuven, Belgium

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ABSTRACT

In this paper we present a procedure and software allowing to predict and understand device performance by incorporating two dimensional (2D)-carrier profiles obtained from high vacuum scanning spreading resistance microscopy (HV-SSRM) into a device simulator. We demonstrate the incorporation of quantified SSRM 2D-carrier profiles obtained on p-MOSFETs into a device simulator. The simulated electrical characteristics (based on the measured 2D-carrier profiles) of the device show nice agreement with the experimentally obtained device results, whereas calculations based on process simulations with available advanced calibration showed significant discrepancies. With this approach the difficult and time consuming calibration step of the process simulation can be circumvented and device results can be interpreted directly based on the details of the real 2D-carrier profiles.

1. Introduction

As the downscaling in semiconductor industry is continued beyond the 45 nm technology node, correct prediction of device performance using device simulators requires accurate information about the two-dimensional (2D) carrier distribution inside such devices. Therefore, 2D-characterization techniques have become inevitable for dopant/carrier profiling.

High-vacuum scanning spreading resistance microscopy (HV-SSRM) has emerged as a method of reference for 2D-carrier mapping in nanoelectronics devices due to its unique sub-nanometer spatial resolution and high sensitivity ranging from 1×10^{15} to above 1×10^{20} carriers/cm^3 [1–5]. SSRM is an atomic force microscopy based technique used to measure 2D-carrier distributions in semiconductor structures and devices [5,6–8]. In SSRM, a hard conductive tip mounted on an AFM equipped with a logarithmic amplifier is scanned in contact mode over the device to be analyzed (typically along its cross-section) generating 2D-spreading resistance maps that are a direct measure for the local resistivity using calibration curves [9]. Using a high vacuum environment (1×10^{-5} Torr) for SSRM measurements reduces the contaminants and humidity present on the sample cross-section and leads to improved spatial resolution and signal-to-noise ratio [10,11]. Using conversion curves [12,13], taking into account the variations in mobility for different concentrations, materials or dopant species, these resistivity maps can be converted into 2D-carrier distributions. In previous studies it has been demonstrated that 2D-carrier distributions of larger devices (65 nm node) obtained by HV-SSRM can be used to calibrate process simulation tools (TSuprem4) by comparing measured carriers distributions with simulated ones [14].

The use of non-equilibrium dopant activation, incorporation and diffusion phenomena as resulting from processes like plasma doping, milli sec anneal, vacancy engineering, etc. represents a serious challenge for many process simulation tools or is not yet properly incorporated, in particular when considering 2D-interactions. Calibrating these models is also a very time consuming task as one needs to design dedicated experiments (and 2D-measurements) enabling to identify the important parameters for each of the models contained in the process simulators. The latter is a non-trivial task as many of these mechanisms and models are interlinked, such as the various defect-clustering mechanisms, transient diffusion effects, two-dimensional dopant-defect interaction.

To overcome these limitations, we propose in the present work an alternative approach whereby we have developed a procedure and software allowing to directly import the measured 2D-carrier profiles, as measured by SSRM, into the device simulator leading to a fast prediction of device performance. The fact that the device simulator is now using the real 2D-carrier profiles, assuming that in a first approximation it can be used as input for the 2D-active

* Corresponding author at: Imec, Kapeldreef 75, B-3001 Leuven, Belgium.
E-mail address: aftab.nazir@imec.be (A. Nazir).

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dopant profile, rather than some approximate predictions from a process simulator, should also lead to a more accurate prediction and understanding of the device performance.

In this paper we present a comparison between the electrical device characteristics as extracted from the device simulator based on the measured carrier distributions and the actual device data to demonstrate and verify the applicability of such an approach. Section 2 provides the information about experimental details for the devices used in this study. Section 3 explains the implementation of the proposed methodology. This work concentrates on the study of drain-induced barrier lowering (DIBL) which is very sensitive to the lateral gate under-diffusion as well as the doping and the shape of the halo pockets. This assessment and its sensitivity to the quantification details of the SSRM profiles, provides also an in-depth knowledge on the accuracy requirements for the SSRM profiles which are presented in Section 4 of the current paper.

2. Experimental details

The p-MOSFETs studied in this paper were fabricated using a conventional transistor flow with fully silicided (FUSI) gate on a silicon-oxynitride (SiON) gate dielectric. Extension regions were formed after a pre-amorphization step (PAI) with germanium (5×10^{14} cm^{-2}, 20 keV) by boron implantation (7×10^{14} cm^{-2}, 1 keV) and fluorine co-implant (5×10^{14} cm^{-2}, 10 keV). Halo implant was performed with arsenic (3.5×10^{13} cm^{-2} at 40 keV) and boron (3×10^{15} cm^{-2}, 4 keV) was implanted to form the source/drain (HDD) regions. The device structures with different gate lengths were laser annealed (peak temperature of 1350 °C).

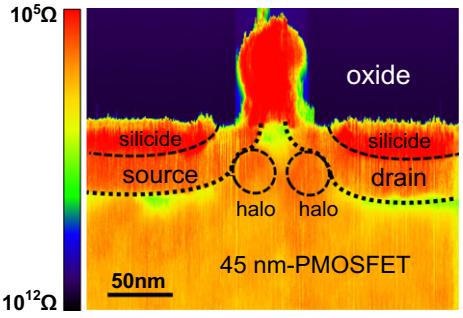

Fig. 1. 2D-spreading resistance distribution of 45 nm P-MOSFET measured by HV-SSRM.

All SSRM measurements were performed using an Enviro-scope system from Bruker. This system has been equipped and modified with the advanced SSRM module to perform the measurements in a HV environment ($\sim 1 \times 10^{-5}$ Torr). In-house fabricated full-diamond tips with a cantilever spring-constant ranging from 3 Nm^{-1} to 10 Nm^{-1} were used to enable/allow measurements with high spatial resolution [3]. The measurements were carried out at a sample bias of +50 mV for optimum performance. A typical example of 2D-spreading resistance distribution measured with HV-SSRM of a 45 nm p-MOS device is presented in Fig. 1.

3. Implementation of proposed methodology

A schematic illustration of the proposed framework is presented in Fig. 2a. The raw data (2D-spreading resistance distribution) of the actual devices were acquired with HV-SSRM. The obtained 2D-spreading resistance maps were then imported into an in-house built software (MicroQuanti) along with p- and n-type calibration curves in order to quantify the measured results, i.e. to perform the conversion from spreading resistance towards active dopant concentration. In this conversion standard mobilities [12,13] as a function of dopant concentration are used. However, provisions are made to import alternative relations if they would be available for a specific process/material. The resulting 2D-carrier distributions are then imported into the device structure defined in process simulator SProcess/TSuprem4 [15]. Note that at present we set the SSRM-carrier distribution equal to the active dopant distribution ignoring the effects of the mobile carrier diffusion on the observed junction depths. A correction for the latter, to be implemented at a later stage, does require the backward solution of the 2D-Poisson equation. However we have assessed the error for the case shown in Fig. 6a by calculating the mobile carrier distribution starting from the active dopant profile extracted from the process simulation (red curve in Fig. 6a). The results show that

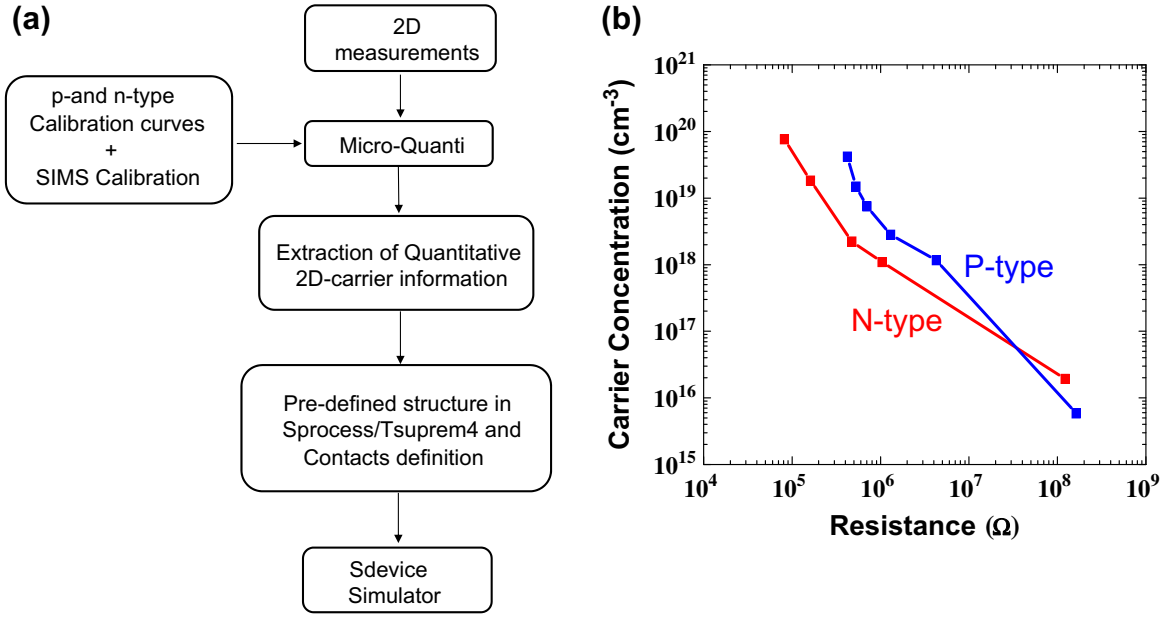

Fig. 2. (a) Schematic illustration of the framework for the integration of SSRM carrier maps into the device simulators. (b) Calibration curves for p- and n-type silicon obtained from HV-SSRM measurements on dedicated calibration staircase structures to convert spreading resistance to carrier concentration.