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Two-stage trigger silicon-controller rectifier (SCR) for radio-frequency (RF) input and output protections in nanometer technologies

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ABSTRACT

In this paper, a two-stage trigger (TST) scheme is proposed to implement a low-capacitance and zero-ohm input resistance electrostatic-discharge (ESD) protection device for nanometer technology applications. Besides the main trigger device diode string, the output transistor can also be used as the trigger device. The dimension of the main trigger device can be reduced for minimizing its capacitance with the additional trigger device. Moreover, the output transistor can be as the driving device without any series resistor. This is because the diode string can help to prevent integrated circuits (ICs) from ESD damage before the primary ESD protection device turns on.

1. Introduction

CMOS technology scaling has resulted in a continuous improvement in radio-frequency (RF) performances of MOSFETs. The cut-off frequency (f_T) over 100 GHz has been demonstrated in the 90 nm CMOS technology [1]. In order not to interfere with the RF signal, a transistor has the maximum loading capacitance limitation [2] and cannot be in series with the resistor. This is because the series resistor will induce the noise, reflection, and increase the power gain loss. Ideal ESD devices for RF input and output protections not only should be low-capacitance devices but also should be zero-ohm resistance devices. With the move into nanometer technologies, however, devices become more vulnerable to the ESD stress than ever due to the ultra-thin oxide (<20 Å), ultra-shallow junction, and short-channel effect [3]. How to develop low-capacitance ESD protection devices to protect the vulnerable output transistors without any series resistors becomes a big challenge in nanometer CMOS technologies.

Although several schemes [4–6] have been demonstrated that allow the RF signal pad to connect the drain or gate of the transistor directly, they all have their own limitations. The diode trigger silicon-control-rectifier (DTSCR) [4] has been demonstrated that can protect the ultra-thin oxide in nanometer technologies. However, its ESD protection capability for the core device (1.0 V) is still unknown. The mutual-protection (MP) scheme [5] is a scheme to enhance the device ESD robustness. Using this scheme, the ESD threshold voltage of output transistor strongly depends on its size. Without enough dimensions, the output transistor cannot own the required ESD level even the MP scheme is used. The semi-self-protection (SSP) scheme [6] is only verified in 0.18 um technologies. However, the maximum current density of the fully silicided transistor decreases from 5.3 mA/μm to 1.3 mA/μm as the technology switches from the 0.18 μm process to the 45 nm process (Fig. 1). Because of lacking the enough self-protection capability, the output transistor's ESD capability by using the SSP scheme is still questionable in nanometer technologies.

In [5], the MP scheme can be used to improve the ESD performance of the output transistor to compensate its self-protection capability decrease. In [6], if the self-protection capability of the output transistor is recovered, the SSP scheme still can work well in nanometer technologies. From the above, a new ESD structure, which combines MP and SSP schemes, is proposed for RF output protection in nanometer technologies [7]. Since the new ESD structure includes two different kinds of trigger devices and one primary ESD device (SCR), it is called two-stage trigger (TST) ESD protection device.

In this work, the DTSCR, SSP-ESD device and TST-ESD device are investigated by using the 45 nm technology to study the influence of the trigger device on the protection capabilities of these ESD devices for core devices.

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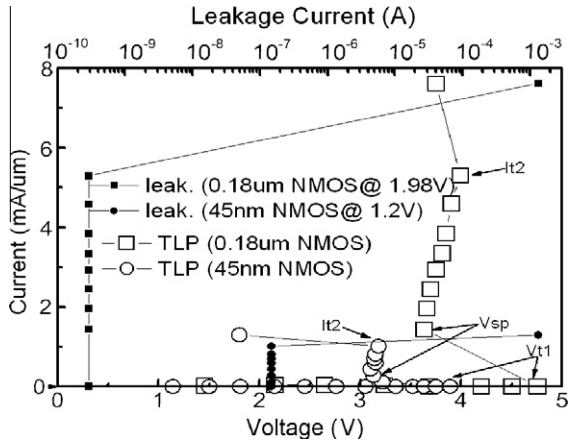

Fig. 1. High current IV characteristics of fully silicided NMOSFET for 0.18 μm and 45 nm technologies.

2. Device structures

The process used to fabricate the devices is the 45 nm CMOS technology in 1.0 V/1.8 V and all devices are applied only for 1.0 V operations with 16 Å gate oxide thicknesses. In this study, the main difference of the three test structures is the trigger device. For positive ESD stresses, all test structures use the SCR as the primary ESD protection device; for negative ESD stresses, the diode (D_A) from the *n*-type well (NW) to P-substrate is applied. All the three test structures are shown in Figs. 2, 5, and 8, respectively. In addition, there is a P+ guard-ring, an NW guard-ring and one power clamping protection device between the power terminal (V_{CC}) and the ground terminal (V_{SS}). Combined with the two guard-rings and power clamping device, all test structures can provide ESD protections for ESD four different zapping modes [6].

2.1. Diode-trigger SCR (DTSCR)

Fig. 2 shows the layout and schematic diagrams of the DTSCR [4] and one output NMOSFET transistor in 64 μm total channel width. The DTSCR has one kind of trigger device, which is three-stage diode strings (TSDSs) in parallel and located at outside the primary ESD protection device (SCR). If the applied voltage is higher than the turn-on threshold voltage of the TSDS, the diodes act as the pnp bipolar transistors (D1–D3 in Fig. 2b) to inject the emitter currents into the P-substrate to raise the substrate potential. As the potential voltage (V_{sub}) of the under-SCR cathode-substrate is raised higher than 0.7 V, the p–n junction between the cathode and P-substrate is forwarded to cause the npn bipolar (npn_s) turn on. Thus, electrons injected from the npn_s are collected by the SCR anode to pull down the NW potential (V_{NW}) to induce the pnp bipolar (pnp_s) turn on. When both npn_s and pnp_s turn on, the SCR enters the latch-up state [8] (SCR turns on).

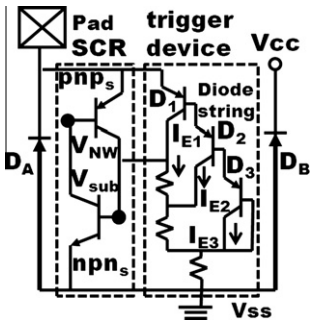

Fig. 2b. The schematic diagram for DTSCR.

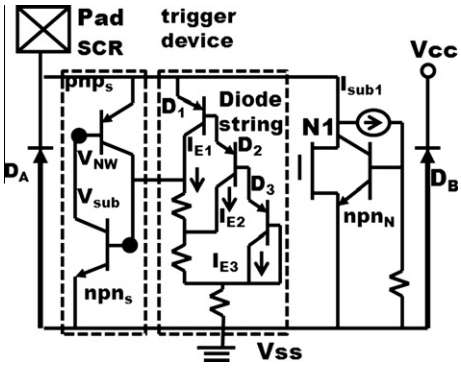

Fig. 2c. The schematic diagram for DTSCR with output transistor (N1).

Fig. 3 shows the high current IV characteristics of the DTSCR (Fig. 2b) under the 100*n* s transmission line pulse (TLP) stress events. The trigger-on voltage (V_{t1}), the snapback voltage (V_{sp}) and the maximum current before damage (secondary breakdown current, I_{t2}) of the DTSCR are 4.4 V, 1.6 V and 1.42 A, respectively. If the device leakage current (Leak.) reaches 1 μA, the device status is decided as FAIL. Before the failure, the device current is I_{t2}. Fig. 4 shows the high current *I–V* characteristics of only N1 and DTSCR combined with the clamping device N1 (Fig. 2c). Both devices are under 100*n* s TLP stresses. V_{t1}, V_{sp}, I_{t2} of DTSCR with N1 are similar to those of N1, but much different from those of DTSCR (Fig. 3). This implies that DTSCR cannot be turned on for protecting N1 since its V_{t1} is larger than N1's V_{t1} (3.95 V). From ESD test results, DTSCR can pass HBM 2.5 KV and MM 100 V. However, DTSCR with N1 cannot pass HBM 500 V or MM 50 V.

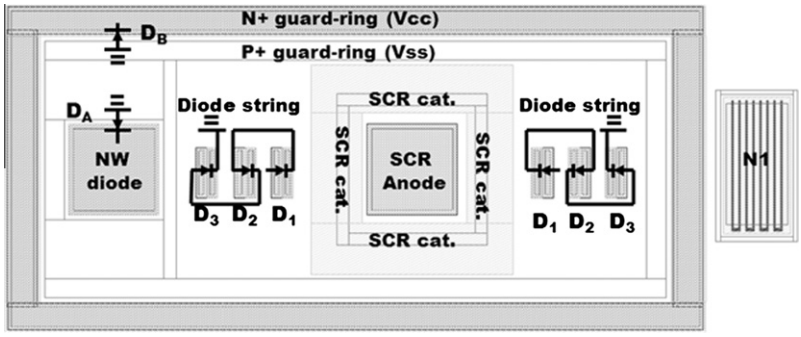

Fig. 2a. The layout of DTSCR with the output transistor (N1).