Solid-State Electronics 70 (2012) 33–38

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

CMOS without doping: Multi-gate silicon-nanowire field-effect-transistors

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ARTICLE INFO

Article history:
Available online 1 December 2011

Keywords:
Silicon nanowire
Π-Gate
Mid-gap Schottky-barrier
Dopant-free

ABSTRACT

In this paper, we report on the fabrication and characterization of voltage configurable nanowire field-effect-transistor (NWFET) devices suitable to broaden the flexibility in circuit design, e.g. for reconfigurable logic. Silicon NW-structures with mid-gap Schottky source and drain (S/D) junctions on silicon-on-insulator (SOI) substrate have been fabricated as unipolar complementary metal–oxide–semiconductor (CMOS) transistors. The desired device type, i.e. NMOS or PMOS, is selected by applying an appropriate back-gate bias. The programming capabilities of the devices fabricated using this approach are demonstrated experimentally using a freely configurable CMOS-NWFET inverter circuit on a MultiSOI-substrate like set-up.

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1. Introduction

Silicon nanowires are intensively studied by many research groups and considered as a promising replacement for standard planar MOSFET based transistor technology, since classic geometric downscaling of the MOSFET devices dimensions is approaching critical physical barriers and is reported to come to an end, eventually [1]. However, the ambipolar [2] nature of the nanowires turns out to be a roadblock, as unipolar p-type and n-type transistors are necessary for a CMOS inverter, the basic building block for today's logic circuits [3]. Problems concerning bottom-up fabrication methods, e.g. vapor–liquid–solid processes and their compatibility to standard CMOS fabrication procedures [4] would be circumvented by the fabrication of top-down fabricated unipolar nanowire devices, using Schottky-barrier (SB) contacts for source and drain metallization. Moreover, in our proposed concept device-doping is replaced by the back-gate control-voltage, leading way to select the transistor-type (i.e. PMOS or NMOS) on the fly. In terms of fabrication, a standard top-down technology has been used, forming the nanowire by means of e-beam lithography and subsequent reactive ion etching. Fig. 1 gives a schematic view of the nanowire structure on a standard SOI substrate. The full potential of the device technology is expected on MultiSOI [5] substrates, basically consisting of two SOI substrates stacked on top of each other. The first (buried) silicon layer acts as the back-gate contact for each NWFET, the top-silicon contains the active area of the device, i.e. the nanowire itself. However, for the reason of cost and simplicity we implemented our logic gate on conventional SOI substrates in order to verify the process concept and demonstrate device functionality.

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doi:10.1016/j.sse.2011.11.011

2. Device fabrication

The devices are fabricated on ultrathin-body SOI substrates with a top-silicon thickness of 70 nm, a buried-oxide thickness of 145 nm and a low boron doping level of 10^{15} cm^{-3}. Note, that no undoped SOI is currently available. First, alignment marks are generated for the subsequent electron beam lithography (EBL), by which 80 nm wide silicon fins are being patterned into a negative resist and subsequently transferred into the top-Si layer via reactive ion etching using a state-of-the-art hydrogen-bromide plasma. The gate-oxide is formed by means of dry thermal oxidation at 1000 °C in a horizontal tube furnace, leading to a gate-oxide thickness of 8 nm. Contact holes are patterned via EBL and opened by wet chemical etching in hydrofluoric acid. The contact pads are structured using a double-layer lift-off resist process. Metallization is performed by electron beam evaporation of 70 nm nickel capped with 180 nm aluminum. All front-gate contacts and electrodes are formed in the same way. Subsequently the source and drain contacts are silicided using a so-called forming gas composition. During this heat treatment, the nickel reacts with the silicon surface forming mid-gap Schottky-barrier contacts [6] to the low-doped silicon nanowire. The total width of the oxidized silicon fin is measured to 105 nm by scanning electron microscopy (SEM). When the silicon-oxide thickness is subtracted the resulting width of the silicon fin is 90 nm. The total height of the oxidized silicon fin is measured to 60 nm with atomic force microscopy (AFM), corresponding to silicon height of 52 nm. The gate to source distance and the gate to drain distance amounts to 20 μm and the width of the each contact is 5 μm. Note, that during the entire fabrication no additional doping is required, making this process independent of issues arising in modern MOSFET fabrication, i.e. statistic dopant fluctuation, lightly doped drains, halo implantations and more. Fig. 2 shows cross-sectional SEM (XSEM) images

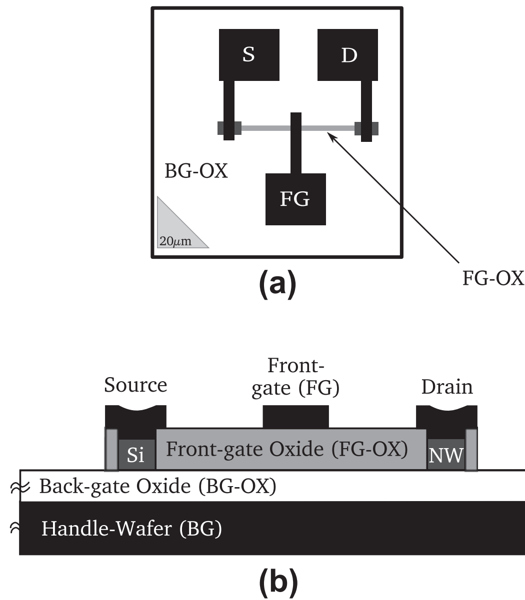

Fig. 1. (a) Topview of the nanowire-FET (NWFET) layout. (b) Cross-section through a Π-front-gate NWFET on silicon-on-insulator (SOI) material.

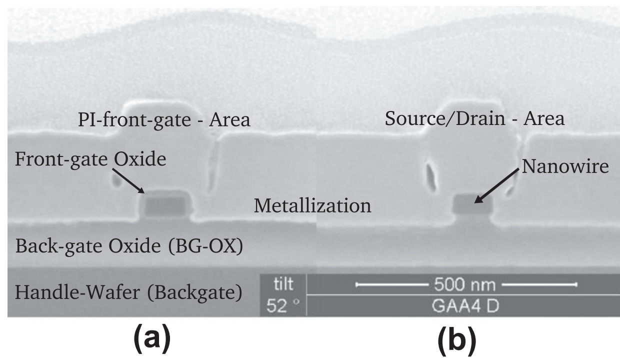

Fig. 2. (a) Cross-sectional SEM (XSEM) picture of the NWFET's Π-front-gate area. (b) XSEM of the corresponding NWFET's source and drain (S/D) region.

to illustrate the gate area with its tri-gate structure and the S/D area, respectively.

3. Results and discussion

3.1. Back-gate control

In Fig. 3 the control of the back-gate over the nanowire channel is observed in linear and logarithmic scales for two voltages of V_{DS}. Application of a sufficient negative bias V_{BG} to the back-gate electrode accumulates holes in the channel region, and due to the S/D-bias a hole current flows. Changing the polarity of the back-gate voltage to positive polarity, electrons are accumulated and an electron current is observed. This behavior is not affected by the low p-type doping of the used SOI-substrate, the channel charge carriers are supplied by mid-gap SB S/D-contacts. This kind of device behavior can be considered as an enhancement mode transistor operation. Fig. 4 schematically shows the working principle of the back-gate control for hole (Fig. 4a) and electron enhancement (Fig. 4b), respectively. For $V_{BG} \ll 0$ V the valence-band is pushed above the Fermi-level of the SB contacts (ϕ_M). The band-bending at the metal–semiconductor interface allows carriers to tunnel into the valence-band, and therefore holes start

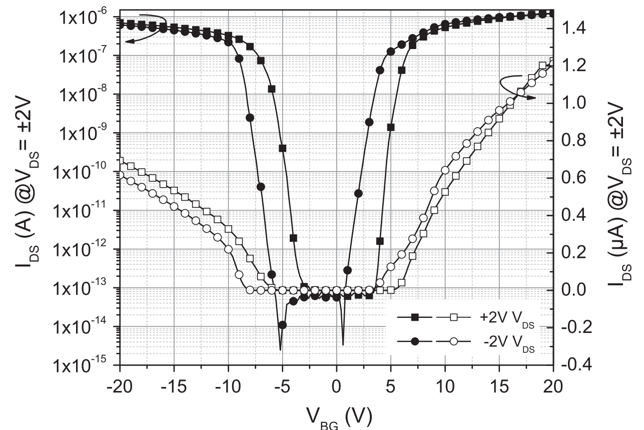

Fig. 3. Sub-threshold characteristic of the back-gate electrode at floating front-gate configuration with different S/D-voltage $V_{DS} = \pm 2$ V on logarithmic scale (filled symbols, left *y*-axis) and linear scale (open symbols, right *y*-axis).

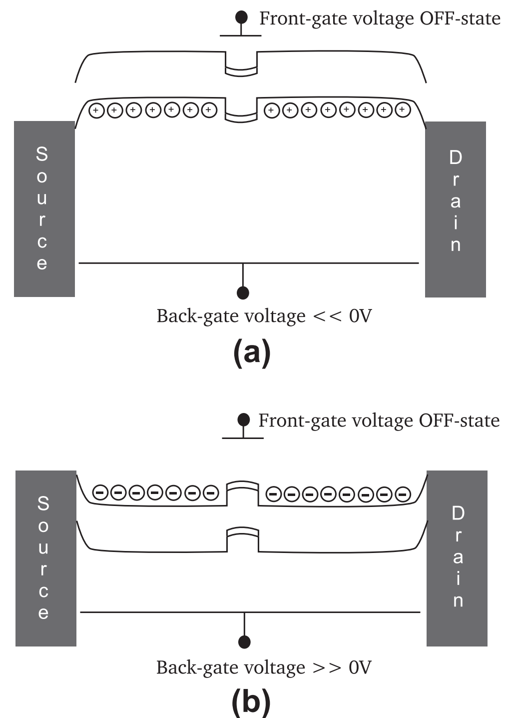

Fig. 4. Schematic band-diagram of the front- and back-gate control of the NWFET within the channel region for the OFF-state. (a) Accumulation of p-type carriers (holes) at the BG-OX/top-Si interface: $V_{BG} \ll 0$ V, $V_{DS} = 0$ V. (b) Accumulation of n-type carriers (electrons) at the BG-OX/top-Si interface: $V_{BG} \gg 0$ V, $V_{DS} = 0$ V.

to fill the valence-band. The opposite case occurs by application of $V_{BG} \gg 0$ V, the conduction-band edge is drawn below ϕ_M and electrons are capable to populate the conduction-band. In the schematic band-diagram in Fig. 4 the front-gate voltage is assumed to be in the OFF-state. The tunneling of the charge carriers from the Schottky-barriers is confirmed by current measurements at elevated temperatures as illustrated in Fig. 5. The ON-state current decreases with raising temperature. This decrease is related to the decrease of charge carrier mobility with rising temperature, indicating that according to theoretical considerations [7] field emission (i.e. tunneling) of carriers into the semiconductor is the dominant mechanism.

Accordingly, the back-gate enhancement mode transistor is responsible for providing the predominant charge carrier type

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