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FinFlash with buried storage ONO layer for flash memory application

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ABSTRACT

Advanced FinFETs fabricated on alternative SOI substrate with SiO_2–Si_3N_4–SiO_2 (ONO) buried insulator are investigated for flash memory applications. The Si_3N_4 buried layer can easily trap charges by applying high back-gate or reasonable drain bias. The shift of the drain current, flowing at front-gate interface and resulting from interface coupling, indicates the amount of trapped/detrapped charges in the buried nitride layer. The memory effect, which is defined as the difference of drain current level, is induced by trapped/detrapped charges. The trapped charges in the buried dielectric also induce a drain current hysteresis when the back-gate bias is dynamically scanned. Systematic measurements reveal that the memory effect depends on the bias conditions and geometrical parameters.

1. Introduction

Advanced SOI devices with alternative buried insulator (BOX) are investigated for several applications: self-heating reduction [1], strain transfer [2], fin etch definition avoiding undercut [3] and non-volatile charge storage [4,5]. In this work, we studied advanced FinFETs fabricated on SOI with multi-stack SiO_2–Si_3N_4–SiO_2 (ONO) buried insulator, for innovating flash memory application with remote charge trapping.

Until now, various architectures of flash memory cell have been proposed. The conventional flash memory cell with a floating gate for charge trapping is the most widely used structure [6]. In the case of floating gate structure, the charge trapping interface and the conduction interface are located within the same gate. For this reason, the trapped charges in the floating gate are disturbed during reading operation.

For the further evolution of flash memory cell, one of the most important issues is the cell downscaling. Beyond the 22 nm technology node, the channel length and the tunneling oxide thickness reduction will cause several critical problems. Shorter gate length, which requires thinner tunneling oxide to control the device, could compromise the reliability of the device and the flash memory function. Thinner tunneling oxide improves the device controllability and allows faster programming/erasing time and smaller operating bias. But, the reduction of the tunneling oxide induces a degradation of the retention time. Another important problem linked to high operating bias is the wasted silicon area used for the co-integration.

A silicon–oxide–nitride–oxide–silicon (SONOS) structure, where the nitride film is used for charge storing, was proposed [7]. Usually, the SONOS device is made by stacked layers on Si substrate. The SONOS flash memory cell is attractive because the device fabrication process is simple and the nitride charge trapping layer provides good retention time. For these reasons, the SONOS devices are very promising candidates for flash memory cells.

For flash memory application, the FinFlash with ONO buried storage layer may need more complex control circuit and slightly larger silicon area if the second gate is used. Nevertheless, this device has definite merits. The key advantage of FinFETs with ONO buried layer is that analog/logic and memory operations can be carried out within the same cell due to the decoupling of the storage and read operations. Another benefit of this technology is the separation of the programming interface from the reading interface. The charges are trapped in the nitride buried layer and sensed at the front-gate interface. The separation of the two interfaces improves the reliability of the memory device and reduces charge disturbance problems.

In this paper, we will show that the Si_3N_4 buried insulator can efficiently trap charges in FinFlash devices fabricated on ONO buried insulator. We will also introduce two different programming/erasing mechanisms. One is the carrier tunneling by applying high back-gate bias and the other is the carrier injection by moderately high drain biasing. The memory effects are induced by trapped charges in the Si_3N_4 buried insulator. The drain current hysteresis due to charge trapping/detrapping will be studied by scanning the

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back-gate bias. The experimental results will be reported for different bias conditions and geometrical parameters.

2. Device fabrication

SOI wafers with $SiO_2/Si_3N_4/SiO_2$ multi-layer buried insulator were used as starting material. Wafers with ONO buried layer were fabricated with the Smart-Cut™ technology. The SiO_2 (2.5 nm), Si_3N_4 (20 nm) and SiO_2 (70 nm) layers were stacked, from top to bottom. Si_3N_4 is an appropriate material for flash memory application, but $Si–Si_3N_4$ interface degrades the transistor performance [3]. This is why the Si_3N_4 buried layer was sandwiched within two SiO_2 layers. The upper SiO_2 layer is very thin (2.5 nm) and enables carrier tunneling. The Si film thickness was 65 nm which defined the fin height. Hydrogen annealing was performed to smooth the fin sidewalls. The front-gate oxide thickness is 1.8 nm. TiSiN grown by LPCVD was used as gate material. The fabrication was completed with conventional CMOS process modules.

To investigate the effects of geometrical parameters, FinFETs with variable gate lengths L_G and fin widths W_F were formed. The finished devices have fin widths narrower by about 45 nm than the masked-defined widths. The number of fingers N_F connected in parallel varies from 1 to 100. All devices operate in full depletion mode. Fig. 1 shows the structure of the SOI FinFETs fabricated on the ONO buried layer.

3. Charge trapping in the Si_3N_4 buried layer

The Si_3N_4 buried layer can trap charges according to the bias condition or fabrication process. These trapped charges in the nitride buried layer change the device characteristics such as threshold voltage, mobility and so on [8]. In Fig. 2, we compare the

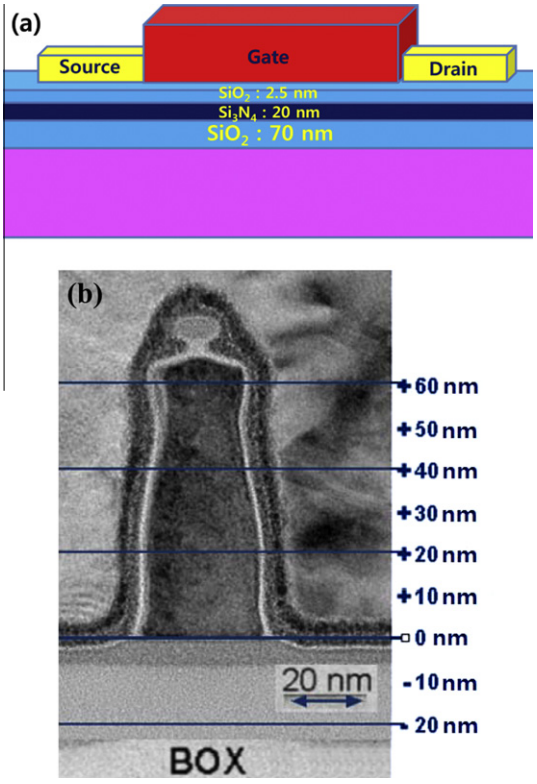

Fig. 1. (a) Structure and (b) TEM cross section of SOI FinFET with ONO buried insulator. The buried insulator features SiO_2 (2.5 nm), Si_3N_4 (20 nm) and SiO_2 (70 nm) layers, from top to bottom.

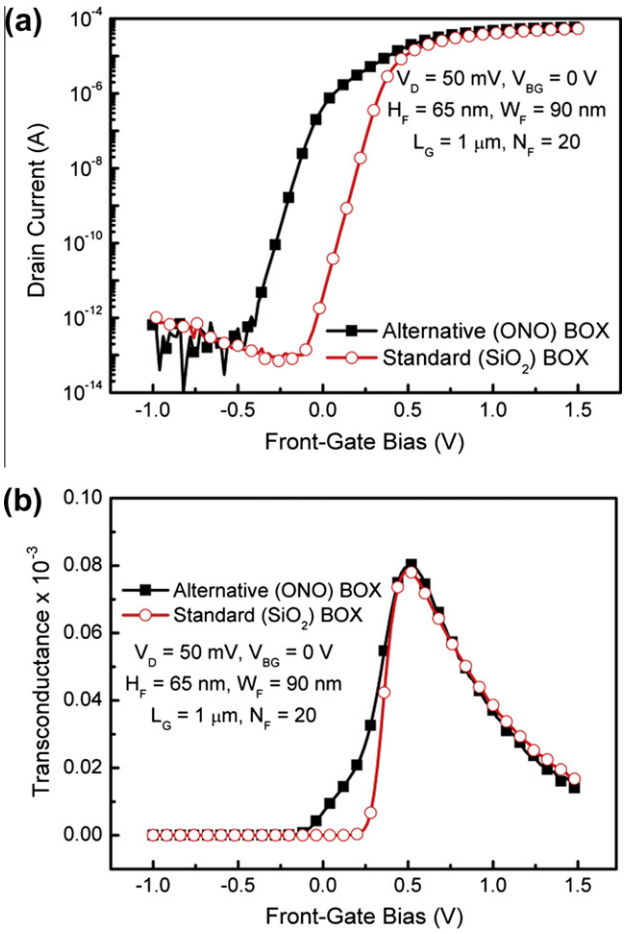

Fig. 2. Comparison of (a) drain current and (b) transconductance characteristics between FinFETs with standard (SiO_2) buried insulator and alternative ($SiO_2/Si_3N_4/SiO_2$) buried insulator.

characteristics of standard SiO_2 buried insulator (BOX) and ONO buried insulator (BOX). In Fig. 2a, the front-channel threshold voltage observed in the ONO BOX MOSFET is lower than in standard SiO_2 BOX devices. During fabrication process, positive charges are trapped in the Si_3N_4 buried layer [3]. Therefore, the body potential is increased and the front-channel threshold voltage is decreased by these positive trapped charges.

In Fig. 2b, we can see a hump in the transconductance curve around $V_{FG} = 0$ V. This hump arises from the activation of the FinFET back-channel which can be easily turned on by positive trapped charges in the Si_3N_4 buried insulator. This explains why the parasitic back-channel and the hump in the transconductance curve are observed only for the ONO FinFET. The parasitic channel leads to a lateral shift of the subthreshold characteristics of Fig. 2a (~450 mV), larger than the actual shift of the front-channel threshold voltage (~150 mV).

History effects are generated by back-gate bias V_{BG} higher than ±15 V. In Fig. 3, $I_D(V_{FG})$ curves are measured for different back-gate biases. The back-gate voltage is consecutively changed in the following sequence: 0 V, +15 V, 0 V, −15 V and 0 V. The front-channel threshold voltage V_{THF} is decreased by using a positive programming back-gate bias (+15 V) due to the electrostatic coupling between the gates. Therefore, the drain current curve shifts to the left. By contrast, V_{THF} is increased by applying a negative back-gate bias and the drain curve moves to the right. This behavior reflects the standard coupling effects in Triple-Gate FinFETs [9,10]. The key point is that the $I_D(V_{FG})$ curves are not superposed when measured again at $V_{BG} = 0$ V. This demonstrates that charges are effectively