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# Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling

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ABSTRACT

We report on thin-body tunneling field-effect transistors (TFETs) built on SOI substrates with both $SiO_2$ and $HfO_2$ gate dielectrics. The source–drain leakage current is suppressed by the introduction of an intrinsic region adjacent to the drain, reducing the electric field at the tunnel junction in the off state. We also investigate the temperature dependence of the TFET characteristics and demonstrate that the temperature-induced change in the Si bandgap is the main mechanism that determines the tunneling barrier and hence the drain current $I_D$. We present a model of the TFET as a combination of a gated diode and a MOSFET, which can be solved analytically and can predict the experimentally measured $I_D$ over a wide range of drain and gate bias. Finally we report on the low frequency noise (LFN) behavior of TFETs, which unlike conventional MOSFETs exhibits $1/f^2$ frequency dependence even for large gate areas. This dependence indicates less trapping due to the much smaller effective gate length over the tunneling junction.


## 1. Introduction

As the scaling of conventional CMOS devices is hampered by short-channel effects (SCEs), silicon-compatible devices based on different principles are being studied for their unique properties. In particular, the tunneling field effect transistor (TFET) [1] is of interest due to its complete semiconductor process compatibility and similarity of device layout with the Si MOSFET. The current in TFETs is carried by band-to-band tunneling (BTBT), which makes it theoretically possible to reach extremely low off-state currents ($I_{OFF}$) as well as an ultra-low subthreshold slope ($S$) below the ideal MOSFET value of 60 mV/decade at room temperature. A number of studies have focused on power consumption in TFETs, reporting a theoretical advantage over standard MOSFETs [2,3]. In order to enhance the on-state current ($I_{ON}$), multigate [4] and lower bandgap semiconductors, such as Ge and SiGe, have been reported [5–9]. At the same time, experimentally realized TFETs have typically suffered from difficulties in simultaneously achieving low $S$ and high $I_{ON}$, as well as from high source–drain leakage current ($I_{LEAK}$) due to ambipolar conduction, especially for low bandgap semiconductors.

In addition to experimental demonstrations, analytical TFET models are important for understanding device physics (including BTBT and leakage effects) and quick prediction of device performance [10–12]. In previously reported models, the channel was assumed to be fully depleted, which suppresses [11] or minimizes [12] the effect of drain voltage $V_D$ on the tunneling junction, especially at high gate voltage $V_{GS}$ in long-channel TFETs. Furthermore, ignoring the carrier transport in the channel also removes the current saturation mechanism of future TFETs with higher $I_{ON}$.

In this work, we focus on several aspects of Si TFETs. First, we compare TFETs with $SiO_2$ and $HfO_2$ gate dielectrics to demonstrate lower $S$ and higher $I_{ON}$ in devices with thinner equivalent oxide thickness (EOT). Second, an asymmetrical TFET layout with an intrinsic region ($L_{IN}$) at drain side is demonstrated to effectively suppress $I_{LEAK}$ while retaining the same $I_{ON}$. These experimental results are confirmed using device and process simulations based on Silvaco TCAD. Third, temperature variation tests are performed to examine the validity of Kane's model [13] of the BTBT process. Further, an analytical model of TFET including a MOSFET channel component is proposed. While this model requires numerical evaluation over the entire range of bias and current, it reduces to a compact and convenient form for our experimental TFETs with relatively low $I_{ON}$. Finally, we present low-frequency noise (LFN) measurements on TFETs and qualitatively explain the different LFN properties of TFETs compared to standard MOSFETs (where LFN measurements are widely used to extract trap properties [14,15]).

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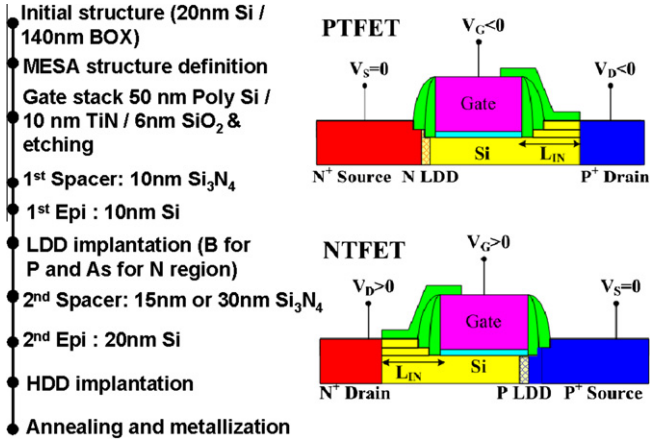


**Fig. 1.** Fabrication process flow and bias polarity of TFETs. In PTFET, the gate is negatively biased and the BTBT occurs at the n+ doped source. Conversely, in NTFET, the gate is positively biased and the BTBT occurs at the p+ doped source.

## 2. Fabrication and device structure

### 2.1. Fabrication process

Our TFET fabrication sequence is completely compatible with fully depleted SOI CMOS process flow. The process started from an SOI Unibond substrate with 140 nm BOX and 20 nm active Si layer. The isolated device active areas (mesa structure) were formed by photolithography and dry etching, followed by the definition of gate stack which is composed of three layers, as illustrated in Fig. 1. Two different gate oxides were formed for comparison: either a 6 nm $SiO_2$ grown by dry oxidation or a 3 nm ALD-deposited $HfO_2$. After the deposition of a metal gate (10 nm TiN), 50 nm thick polysilicon was deposited for silicidation. The first spacer was formed by the deposition of 10 nm $Si_3N_4$ in LPCVD, then a 10 nm Si layer was epitaxially grown by CVD process. The N-type LDD was formed by implantation of As with dose of $1 \times 10^{15}$ $cm^{-2}$ and energy of 9 keV, while $BF_2$ implantation with dose of $1 \times 10^{15}$ $cm^{-2}$ and energy of 7 keV was used for formation of P-type LDD. Then, a second spacer of 15 or 30 nm and a Si layer of 20 nm were deposited. Before the implantation of N-HDD and P-HDD regions, a $Si_3N_4$ layer was formed to protect the intrinsic region $L_{IN}$. The dose and energy of As for NHDD implantation were $2 \times 10^{15}$ $cm^{-2}$ and 20 keV, respectively, whereas, for PHDD implantation, these values were $3 \times 10^{15}$ $cm^{-2}$ and 5 keV. Rapid thermal annealing (RTA) was used to activate the dopants, followed by the metallization.

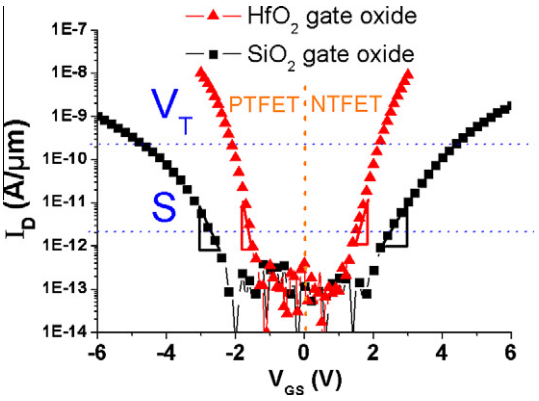


**Fig. 3.** Measured $I_D$–$V_{GS}$ curves of both NTFETs and PTFETs based on different gate oxides ($L_G$ = 400 nm, $|V_{DS}|$ = 1 V). The inset symbols show the definitions of $V_T$ and $S$.

### 2.2. Device structure

The structure of the fabricated TFETs is quite similar to that of a MOSFET with double spacers and raised S/D, shown in Fig. 2a. The only structural difference between TFETs and MOSFETs lies in the opposite doping of the TFET source and drain. Furthermore, for suppressing the ambipolar current, the structure of some TFETs was rendered asymmetrical by adding an intrinsic region $L_{IN}$ separating the drain contact from the channel as shown in Fig. 2b.

For simplicity, the N+ region in a PTFET is defined as source while the P+ region is defined as drain. The opposite definition applies to NTFETs, as shown in Fig. 1. The source of both PTFETs and NTFETs is always grounded, while the drain is negatively biased in PTFETs and positively biased in NTFETs. The $I_{ON}$ is produced by tunneling at the source-channel junction at $V_{GS} < 0$ for PTFETs and $V_{GS} > 0$ for NTFETs.

## 3. Electrical characterization and analysis

The fabricated devices were systematically characterized. From $C$–$V$ measurements, the EOT values of TFETs with 6 nm $SiO_2$ and 3 nm $HfO_2$ gate oxides were 6 nm and 2.2 nm, respectively. The gate width of all TFETs was 10 μm, the gate length $L_G$ varied from 100 to 400 nm, and the intrinsic region length $L_{IN}$ varied from 0 to 100 nm.

### 3.1. Impact of gate oxide on characteristics

A comparison of $I_D$–$V_{GS}$ curves of NTFETs and PTFETs with different gate oxides and $L_G$ = 400 nm and $|V_D|$ = 1 V is shown in

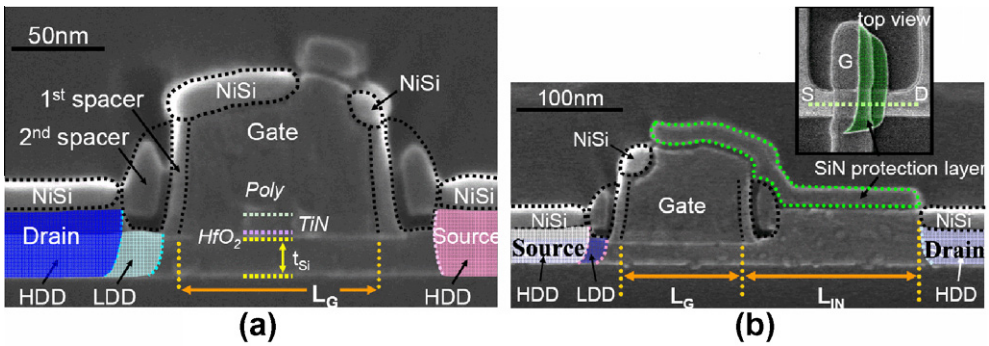


**Fig. 2.** SEM images of fabricated conventional (a) and asymmetric (b) TFETs.