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Research paper

Accidental phase modulation in second-order phase-locked loops

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ABSTRACT

The phase-locked loop, essential element for phase synchronization in communications and control, is studied for several types of application. However, some cases urge for more accurate models, mainly regarding to the accidental phase modulation, an unavoidable phenomenon provoked by imperfections of circuits and transmission media, causing oscillations around the synchronous state, even when this state is reached. In this work, this problem is treated by distinguishing two different cases: jitter (high frequency) and wander (low frequency). In addition, the perturbation origins are modeled, dividing the problem into deterministic and random signal perturbations showing how they affect the equilibrium even with the loop operating in the pull-in range.

1. Introduction

Since proposed by Bellescize in 1932, the phase-locked loop evolved from being a device mounted with discrete electronic components, to being applied in synchronous frequency demodulation systems [1] in different forms of integrated circuits and software implementations, which are present on computational systems, optics communications devices and even in smart-gride applications [2,3].

Clearly, these different applications correspond to different frequency ranges and synchronism accuracy. However, considering that the PLL architecture is always the same, described by a closed loop composed of phase-detector (PD), a low-pass filter (F) and a voltage controlled oscillator (VCO), represented in Fig. 1, there are the following possible adjustments to be considered according to the application [4]:

- PD gain and its linearity.
- F frequency response.
- VCO hold-in range.

The PD is supposed to be nonlinear with the output signal, $v_d(t)$, depending on the sine of the phase difference between the phase of the remote signal, present in the PD input, $v_i(t)$, and the phase of the local oscillation generated by the VCO, $v_o(t)$, from then on, non-small phase errors must be taken into account [5,6].

The filter that integrates the output of the PD will be considered a first-order low-pass lag-lead. The output of the filter, $v_c(t)$, controls the VCO, which its derivative phase is proportional to the filter output [2]. In order to give the results in a

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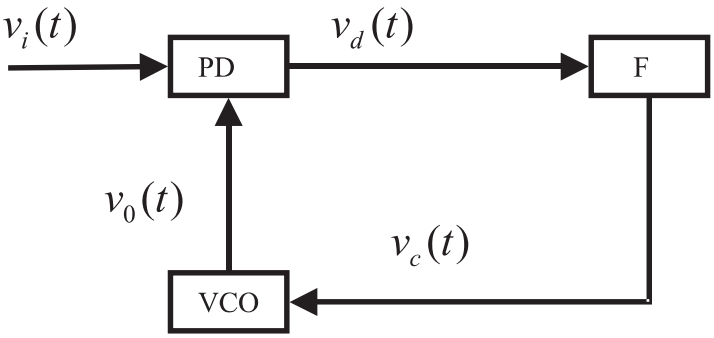

Fig. 1. PLL block diagram.

similar fashion of the classical PLL literature [2], the transfer function of the filter is considered to be:

$$F(s) = \frac{R_2Cs + 1}{(R_1 + R_2)Cs + 1}, \tag{1}$$

with R_1 and R_2 having electrical resistance unit and C, electrical capacitance.

To simplify the notation, some parameters can be defined: $\mu_1 = \frac{1}{(R_1+R_2)C}$, $\mu_2 = K_0K_dV_i$ and $\mu_3 = R_2C$. It can be noticed that μ_1 and μ_2 have frequency units and μ_3 is expressed in time units.

Under these conditions [7], the PLL dynamics is expressed by:

$$\ddot{\phi} + \mu_1(1 + \mu_2\mu_3\cos\phi)\dot{\phi} + \mu_1\mu_2\sin\phi = \ddot{\theta}_i + \mu_1\dot{\theta}_i, \tag{2}$$

with ϕ representing the phase difference between signals $v_i(t)$ and $v_o(t)$, and θ_i the phase of $v_i(t)$.

To normalize the equations, the time t can be replaced by $\tau = \mu_1 t$. Consequently, the dynamics of the second order PLL, for time measured by τ, is given by:

$$\phi'' + (1 + c\cos\phi)\phi' + G\sin\phi = \theta_i'' + \theta_i', \tag{3}$$

with the quotation marks representing the derivatives related to τ, $c = \mu_2\mu_3$ and $G = \frac{\mu_2}{\mu_1}$.

Eq. (3) models the PLL for the several possible θ_i: steps, ramps, parabola and periodic functions, besides its behavior is largely studied.

Some seminal works [2,8,9] present important results about the ideal operation of the PLL, but not considering the accidental phase modulation phenomenon that produces inaccuracies in the clock signal detection, even in the pull-in range [9].

Here, the regular operation of the second-order PLL is presented with a section exploring analytically and numerically its ideal operations in the pull-in range.

Then, the accidental phase modulation is studied, divided into deterministic and random perturbations, with the deterministic case divided into jitter (high frequency) and wander (low frequency) perturbations.

All the simulation work was performed by using MATLAB-Simulink [10] and the models built with its regular blocks. The discussion about the analytical and simulation results is presented in the Conclusions section.

2. Exploring ideal behaviors and the operation in the pull-in range

For different inputs, the possible ideal behaviors are explored by using the analytical results and simulations performed with a Simulink model, built in MATLAB R2013a, with the solving option ode45, i.e., a Dormand-Prince variable step method, with tolerance $1,0.10^{-9}$ [10].

As the main function of the PLL is to synchronize the phase of the VCO output (θ_o) with the phase of the PD input (θ_i), the dynamics of the phase error ϕ is analyzed, for different phase inputs θ_i.

2.1. Phase step

A typical PLL phase input is the step, applied at $t = 0_+$. In this case, Eq.(3) is reduced to:

$$\phi'' + (1 + c\cos\phi)\phi' + G\sin\phi = 0. \tag{4}$$

Defining the state $(x_1, x_2) = (\phi, \phi')$, Eq. (4) can be written as:

$$\begin{aligned} x_1' &= x_2 \\ x_2' &= -(1 + c\cos x_1)x_2 - G\sin x_1. \end{aligned} \tag{5}$$