12th IFAC/IEEE Workshop on Discrete Event Systems
Cachan, France. May 14-16, 2014

Maximally Permissive Petri Net Supervisors with a Novel Structure ⋆

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Abstract: This paper presents a novel arc of Petri nets, namely data inhibitor arcs, and its application to deadlock control of discrete event systems. A data inhibitor arc is from a place to a transition labeled with a set of data. The transition is disabled by the place if the number of tokens in the place is in the set of data labeled on the arc. By using the data inhibitor arcs, a maximally permissive Petri net supervisor is designed to prevent a discrete event system from reaching illegal markings. Furthermore, a technique is proposed to find only one control place to make the system live with all legal markings. Finally, we provide examples to demonstrate the proposed approach.

Keywords: Petri net, discrete event system, supervisory control, deadlock, data inhibitor arc.

1. INTRODUCTION

Deadlocks (Coffman et al., 1971) are a constant issue in discrete event systems (DESs) such as flexible manufacturing systems (FMSs), computer systems, communication systems, etc. Petri nets have been widely used to handle deadlocks in DESs due to their compact structures and intuitive representations to model and control these systems. Based on the Petri net analysis technique, a DES is first modeled by a net structure. Then, the property of the system can be analyzed by the Petri net model. Based on the analysis of the model, a Petri net supervisor is designed to avoid the deadlocks. Then, the supervisor can be implemented by computers, programmable logic controllers (PLCs), microcontrollers, etc. In the last decades, there are a lot of work focusing on the liveness-enforcing supervisor according to the Petri net models of DESs (Barkaoui and Abdallah, 1995; Li and Zhou, 2004; Wang et al., 2012).

Reachability graphs can reflect the complete behavior of a Petri net model. Thus, the reachability graph analysis is an important technique in the development of deadlock control of Petri nets since it can always lead to a maximally permissive supervisor. Behavioral permissiveness, structural complexity, and computational complexity are three important criteria to evaluate the performance of a Petri net supervisor. The purpose is to design a net supervisor with maximal permissiveness, simple structure, and efficient computation.

A reachability graph has two partitions: a live zone (LZ) and a deadlock zone (DZ) (Uzam and Zhou, 2006). The LZ includes all legal markings and the DZ contains the illegal markings. For a maximally permissive control purpose, all legal markings should be kept in the controlled system. In (Ghaffari et al., 2003), the theory of regions is applied to design maximally permissive supervisors for Petri net models. They first generate the reachability graph of a Petri net model. Then, the set of marking/transition separation instances (MTSIs) is derived from the reachability graph. An MTSI is a pair of a marking M and a transition t, denoted as (M, t), where M is a legal marking and t is an enabled transition at M whose firing leads to an illegal marking. An MTSI (M, t) can be implemented by disabling t at M. A linear program is used to design a control place to implement an MTSI and all legal markings are kept. Once all MTSIs are implemented, a maximally permissive supervisor is obtained. Huang et al. (2012) propose an approach to improve the computational efficiency of the theory of regions by reducing the number of MTSIs to be considered. In our previous work (Chen et al., 2011), we develop an approach to design maximally permissive control places by forbidding first-met bad markings (FBMs) but no legal markings. An FBM is an illegal marking that can be directly reached by firing a transition at a legal marking. Thus, once all FBMs are forbidden, the system cannot enter the DZ anymore. Then, we can obtain a controlled system that is live with all legal markings. The work in (Chen et al., 2011; Ghaffari et al., 2003; Huang et al., 2012) only considers the maximally permissiveness but no

⋆ This work was supported in part by the National Natural Science Foundation of China under Grant Nos. 61203038 and 61374068, PHC Cai Yuanpei Program 2011 No. 26049WM, the Fundamental Research Funds for the Central Universities under Grant No. JB140402, and the Science and Technology Development Fund, MSAR, under Grant No. 066/2012/A2.

structural complexity. Chen and Li (2011) propose an integer linear programming problem (ILPP) to minimize the number of control places in the obtained supervisor while all legal markings are reachable. That is to say, the obtained supervisor is optimized in both behavioral permissiveness and structural complexity.

There are some Petri net models that cannot be optimally controlled by pure net supervisors. In this case, Chen et al. (2013) propose a maximally permissive supervisor be using self-loops. A self-loop means both an arc from a place to a transition and an arc form the transition to the place. The experimental results in (Chen et al., 2013) show that self-loops are more powerful than pure net models in modeling and controlling a system since it can find maximally permissive supervisors for the net models that cannot be optimally controlled by pure net supervisors.

In this work, we propose a new Petri net structure, called data inhibitor arcs. A data inhibitor arc is an arc from a place p to a transition t with a set of integers labeled on the arc. Then, t is disabled by p at a marking M if $M(p)$ is in the labeled set. Then, we develop an ILPP to design Petri net supervisors with data inhibitor arcs. Experimental results verify that data inhibitor arcs can lead to optimal supervisors for the net models that cannot be optimally controlled by pure net supervisors.

The rest of the paper is organized as follows. Section 2 outlines some basics of Petri nets used throughout this paper. Section 3 presents the definition of inhibitor arcs and the design of optimal supervisors with inhibitor arcs. In Section 4, examples are proposed to illustrate the proposed method. Finally, the paper is concluded in Section 5.

2. PRELIMINARIES

2.1 Petri Nets

A Petri net (Murata, 1989) is a four-tuple $N = (P, T, F, W)$ where P and T are finite and non-empty sets. P is a set of places and T is a set of transitions with $P \cap T = \emptyset$. $F \subseteq (P \times T) \cup (T \times P)$ is called a flow relation, represented by arcs with arrows from places to transitions or from transitions to places. $W : (P \times T) \cup (T \times P) \to \mathbb{N}$ is a mapping that assigns a weight to an arc: $W(x, y) > 0$ if $(x, y) \in F$, and $W(x, y) = 0$, otherwise, where $x, y \in P \cup T$ and $\mathbb{N}$ is the set of non-negative integers. ${}^\bullet x = \{y \in P \cup T \mid (y, x) \in F\}$ is called the preset of x and $x^\bullet = \{y \in P \cup T \mid (x, y) \in F\}$ is called the postset of x. A marking is a mapping $M : P \to \mathbb{N}$. $M(p)$ denotes the number of tokens in place p. The pair (N, M_0) is called a marked Petri net or a net system. A net is pure (self-loop free) if $\forall (x, y) \in (P \times T) \cup (T \times P)$, $W(x, y) > 0$ implies $W(y, x) = 0$.

A transition $t \in T$ is enabled at marking M if $\forall p \in {}^\bullet t$, $M(p) \geq W(p, t)$. This fact is denoted as $M[t\rangle$. Once a transition t fires, it yields a new marking M', denoted as $M[t\rangle M'$, where $M'(p) = M(p) - W(p, t) + W(t, p)$. $M[\rangle$ is the set of all markings reachable from M by firing any possible sequence of transitions. $M_0[\rangle$ is called the set of reachable markings of net N with initial marking M_0, often denoted by $R(N, M_0)$. It can be graphically expressed by a reachability graph. The reachability graph of a net (N, M_0), denoted as $G(N, M_0)$, is a directed graph whose nodes are markings in $R(N, M_0)$ and arcs are labeled by the transitions of N.

2.2 Analysis of Reachability Graphs

A reachability graph can be classified into a deadlock-zone (DZ) and a live-zone (LZ) (Uzam and Zhou, 2006), where the DZ contains all illegal markings and the LZ contains all legal markings. The set $\mathcal{M}_L$ of legal markings is $\mathcal{M}_L = \{M | M \in R(N, M_0) \wedge M_0 \in R(N, M)\}$. An MTSI is a pair of a marking M and a transition t, denoted as (M, t), whose set is defined as $\Omega = \{(M, t) | M[t\rangle M' \wedge M \in LZ \wedge M' \in DZ\}$, where M is called a dangerous marking. Let $\mathcal{M}_D$ denote the set of dangerous markings. Removing all dangerous markings from $\mathcal{M}_L$, the rest ones are called good markings, whose set is defined as $\mathcal{M}_G = \mathcal{M}_L - \mathcal{M}_D$.

In the following, we recall some definitions originally from (Chen et al., 2013). Transitions in a Petri net model are classified into two parts: critical and good ones, whose sets are denoted as T_c and T_g, respectively, where $T_c = \{t \in T | \exists M \in R(N, M_0),\ s.t.\ (M, t) \text{ is an MTSI}\}$ and $T_g = \{t \in T | \nexists M \in R(N, M_0),\ s.t.\ (M, t) \text{ is an MTSI}\}$. From a reachability graph, we can see that the liveness can be guaranteed by implementing all MTSIs.

For transition t, a legal marking M is called a t-good marking if t is not enabled at M, or M' with $M[t\rangle M'$ is a legal marking. M is called a t-dangerous marking if M' with $M[t\rangle M'$ is an illegal marking. The sets of t-good and t-dangerous markings are denoted as $\mathcal{G}_t$ and $\mathcal{D}_t$, respectively.

Let t be a transition and M a t-good marking. M is called a t-enabled good marking if $M[t\rangle$. Otherwise, M is called a t-disabled good marking. The sets of t-enabled and t-disabled good markings are denoted by $\mathcal{E}_t$ and $\mathcal{E}_{\bar{t}}$, respectively. Obviously, we have $\mathcal{G}_t = \mathcal{E}_t \cup \mathcal{E}_{\bar{t}}$ and $\mathcal{M}_L = \mathcal{G}_t \cup \mathcal{D}_t$.

Let t be a critical transition and M a t-dangerous marking. (M, t) is called a t-critical MTSI. The set of t-critical MTSIs is denoted as Ω_t. It is easy to have $\Omega_t = \{(M, t) | M \in \mathcal{D}_t\}$.

3. SYNTHESIS OF SUPERVISORS WITH DATA INHIBITOR ARCS

In this section, we propose a new Petri net structure, namely a data inhibitor arc, and its application to optimal deadlock control of Petri nets.

3.1 Data Inhibitor Arc

We first propose the definition of data inhibitor arcs.

Definition 1. A data inhibitor arc is an arc from a place p to a transition t labeled by a set of integers $\{a_1, a_2, \ldots, a_k\}$, denoted as $\mathring{A}(p, t) = \{a_1, a_2, \ldots, a_k\}$, where k is the number of integers in $\{a_1, a_2, \ldots, a_k\}$ and a_i's $(i = 1, 2, \ldots, k)$ are non-negative integers. It is graphically represented by an inhibitor arc from p to t with a label $\{a_1, a_2, \ldots, a_k\}$ on it, as shown in Fig. 1.