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On-chip thermoelectric module comprised of oxide thin film legs

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ABSTRACT

On-chip thermoelectric thin film modules containing 5 legs of *n*-type ($Al_{0.02}Zn_{0.98}O$) and 5 legs of *p*-type ($Ca_3Co_4O_9$) were fabricated on Al_2O_3, $SrTiO_3$ single crystal, and fused silica substrates by pulsed laser deposition technique. Performance of modules was evaluated using ad hoc customized system where the module was set vertically for temperature gradient. The maximum output power (P_{max}) was obtained on Al_2O_3 (0001) single crystal substrate with temperature difference (ΔT) = 230 °C (T_h = 300 °C): P_{max} = 29.9 pW. The value of maximum output power increases with increase of temperature difference (ΔT). These results are encouraging for the practical applications of thermoelectric oxide thin films.

1. Introduction

In the recent years, oxide materials have increasingly gained attention in the thermoelectric community due to their promising characteristics: high stability at high temperatures (600 °C and more), low price, non-toxicity. Consequently, oxides have been started to be regarded as alternative to inter-metallic and alloys for the fabrication of modules to convert waste heat into electricity. Reviews on thermoelectric bulk oxides [1–6] show that the thermoelectric performance is still poor in comparison with metallic materials and requires improvement. The performance of thermoelectric materials is determined by the dimensionless figure of merit $ZT = \sigma \cdot S^2 \cdot T/\kappa$ (S: Seebeck coefficient; σ: electrical conductivity; κ: thermal conductivity; T: absolute temperature) [7].

Still the thermoelectric performance of the best *n*-type bulk oxide $Zn_{0.96}Al_{0.02}Ga_{0.02}O$ (ZT = 0.65 at 1273 K) [8] and the best *p*-type $Ca_{2.8}Lu_{0.15}Ag_{0.05}Co_4O_9$ (ZT = 0.6 at 1100 K) [9] is lower than the benchmark ZT = 1, which is commonly reached by metallic materials (whose generally decompose or become unstable at around 600 °C). Nevertheless, several contributions related to modules based on ZnO as *n*-type material and $Ca_3Co_4O_9$ as *p*-type material have been published [9–11]. Depending on the number of legs and difference of temperature (ΔT), the typical output power (P) of these modules is several milliwatts at high temperatures: P = 3.7–423 mW; ΔT = 260–658 K, T_h (temperature of hot-end of the module) = 773–1100 K, as summarized in [9].

These values are promising and there is a wide room for improvement related to the reduction of high internal resistance of the module and enhancement of the performance of the materials. As a paradigm for any kind of thermoelectric material [12,13], the introduction of nano-sized defects leads to improved phonon scattering, consequently decreasing thermal conductivity and improving ZT [14–18]. This pattern has have been followed successfully in nano-structured BiTe/PbTe multilayers [19], AgPbSbTe alloys embedded with Ag-rich nano-inclusions [20], porous Al-doped ZnO [21], atomically substituted oxides with natural nano-sized precipitates [8,9], nano-engineering [22,23], and many more [24,25]. The main issue is to control the size and distribution of the nano-structures (nano-layers, pores, precipitates, secondary phases) inside the thermoelectric matrix, which have been found quite hard in bulk materials [14–17]. The control of nano-structure and defects in epitaxial thin films through strain engineering and artificial defects are at the advanced stage in several categories of functional oxides such as multiferroics [26], ferroics [27], superconductors [28], electronics [29], and more [30]. This approach is still at preliminary stage in thermoelectric oxide thin films [31].

Anyway, high thermoelectric performance has been reported by various groups in *p*-type [32–34] and *n*-type [35–38] nano-engineered oxide thin films, including our previous reports on Al-doped ZnO [39,40]. The natural consequence is the use of thermoelectric thin films as legs for planar modules. However, to the date, very few reports on fabrication of thermoelectric oxide

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modules based on thin films have been published [41–43]. According to our best knowledge, only one evaluation of thin films module performance was reported: $P = 0.4\ pW/K^2$ in a planar module based on CuO and ZnO legs obtained by sputtering on Al_2O_3 substrate [43].

The aim of this work is to make progress in exploring the field, describing planar modules based on *n*-type ZnO and *p*-type $Ca_3Co_4O_9$ thin film legs fabricated by pulsed laser deposition (PLD) technique. The role of substrate is investigated by evaluating the performance of the module on Al_2O_3, $SrTiO_3$ (STO) and fused silica.

2. Experimental technique

The on-chip thermoelectric module was fabricated by pulsed laser deposition (PLD) technique using Nd:YAG laser (266 nm). Two pellets (20 mm in diameter and 3 mm in thickness) of $Zn_{0.98}Al_{0.02}O$ (AZO) and $Ca_3Co_4O_9$ were prepared by spark plasma sintering and used as the targets in PLD chamber for the thin films deposition.

At first, laser was focused on $Ca_3Co_4O_9$ target and *p*-type legs were deposited on 10 mm × 10 mm substrates by superimposing a custom nickel mask (Ni mask) (Micron Co. Ltd, Osaka) using the following conditions: energy density of about 1.1 J/cm^2; deposition period of 30 min; deposition temperature (T_{dep}) = 700 °C on Al_2O_3 and fused silica substrates, T_{dep} = 650 °C on STO substrates; oxygen pressure of 200 mTorr; laser pulse frequency 10 Hz; substrate-target distance about 35 mm; rotation speed of the target 30% rpm. Optimal deposition temperatures for $Ca_3Co_4O_9$ thin films were chosen after screening from 550 °C to 850 °C: films not showing any X-ray diffraction (XRD) peak were discarded.

Then, Al-doped ZnO (AZO) target was moved under the laser beam and ablated to fabricate n-legs after shifting the custom Ni mask. Conditions used for AZO legs were same as for $Ca_3Co_4O_9$ legs except for higher energy density (about 4.2 J/cm^2) and lower T_{dep} (400 °C on Al_2O_3 substrate, 300 °C on STO and fused silica substrates) as previously tested to produce the best performance thin films. In both steps, the cooling from deposition temperature to room temperature was accomplished in 300 Torr of oxygen. Gold electrodes were sputtered using a custom Ni mask at room temperature after completion of PLD routes in order to achieve the electrical connection of the p–n couples. The sequence of thin film deposition for on-chip thermoelectric module has been shown in Fig. 1(a) along with schematic side view of module. The schematic top view of module and a picture of the module surface are shown in Fig. 1(b) and (c), respectively.

Due to geometrical constraints in some of the characterization facilities, the *n*-type and *p*-type films were prepared separately on small pieces (0.4 × 7 × 0.05 cm^3 slabs) of the three kinds of substrates using the same conditions described above. Structural characterization was performed by XRD (Bruker D8 Discover) and morphology was checked by scattering electron microscopy (SEM) (JEOL, FESEM). The thickness and in-plane roughness were obtained by a Keyence VK-9700 3D microscope. The electrical conductivity was measured in the temperature range 300 K to 600 K by a custom-built four-point-probe technique consisting of a current source (ADCMT 6144), a temperature controller (Cryo-con 32) and a nano voltmeter (Keithley 2182A). Seebeck coefficient

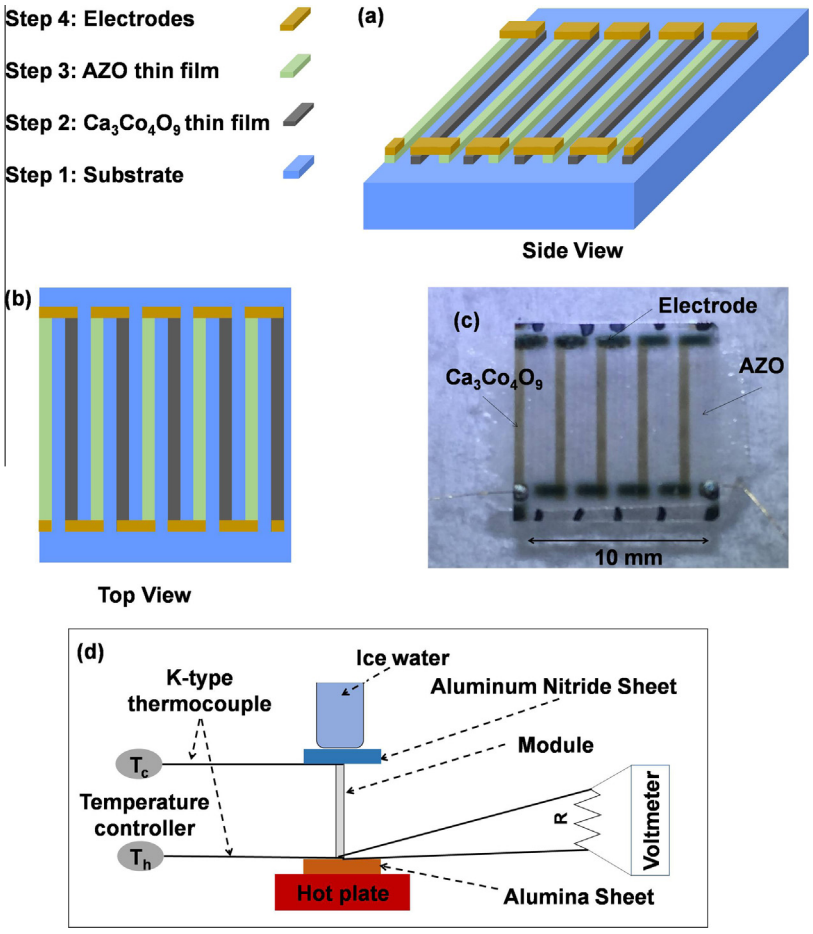

Fig. 1. (a) 3D sketch of the thin film module with sequence of thin films and electrodes deposition; (b) schematic top view of the module and (c) photograph of the module after fabrication of thin films legs and gold contacts; (d) schematic of module testing set-up with a load resistor (*R*).