Reduced-size Signature-based Diagnostic Dictionary for Interconnection Testing

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Abstract: The paper deals with a new and advanced method intended to reduce size of a diagnostic dictionary that is used for detection, localization and identification of static and delay faults in interconnections that are tested with use of ring linear feedback shift registers (R-LFSR). The proposed method assumes that the bus under test comprises n lines and is structured into b fragments with the size of k lines per each fragment. The method also assumes that each of the aforementioned fragments is tested by means of a separate R-LFSR with its length of $2k$ bits. In addition, the paper proposes to subdivide the test procedure into four phases whereas odd and even R-LFSRs are activated alternately. It is the way of subdivision that makes it possible to get rid of the mutual interference between two adjacent R-LFSRs when a short between feedback lines of these neighbouring registers takes place. Likelihood of such interactions was the drawback of previous methods and presented the impediment that prevented the fault dictionary from having its size reduced. The innovative solution that is suggested in this study enables to substantially diminish the dictionary, where its actual size is determined by the multiplicity of r defects within each k-bit part of the connecting bus, even when the bus width $n >> k$.

Keywords: Interconnect test, LFSR, MISR, Ring-LFSR, R-LFSR, Diagnostic dictionary.

1. INTRODUCTION

In general, two types of Interconnect Built-In Self-Test (IBIST) are distinguished, namely test-per-scan IBIST (Koeter and Sparks, 1991), (Su and Tseng, 2001) as well as test-per-clock IBIST (Pedurkar *et al*., 2001), (Jutman, 2004), (Hławiczka *et al*., 2008a, b), (Rudnicki *et al*., 2009), (Hławiczka *et al*., 2009), (Garbolino *et al.*, 2009). Test-per-clock IBIST features two essential advantages over its test-per-scan counterpart: significantly shorter testing time as well as capability of detecting dynamic faults, such as delays in signal timings, crosstalks and many others (Athara and Nourani, 2001).

An interesting type of the test-per-clock IBIST approach based on a special ring register (R-LFSR) was proposed in (Hławiczka *et al*., 2008a, b). It is the structure of the IBIST tester that assumes that n lines of the bus under test is to be used as feedback lines of that R-LFSR register. The cells that are normally used as n transmitters of signals on one side of the bus and n signal receivers on the opposite side of the bus are reconfigured to the test mode and make up a shift register with the length of $2n$ bits. This register together with n lines of the bus under test is actually a ring register (R-LFSR). The register feedback is defined by means of its characteristic polynomial $p(x)$, where non-zero coefficients of that polynomial are associated with bus lines that are incorporated into the feedback structure. During execution of the tests the R-LFSR produces $2n$-bit pseudo-random test vectors. One half of each test vector that presents n of its more significant bits is the test pattern for the interconnecting bus under test.

Studies on these registers (Hławiczka *et al*., 2008a, b) related to application of R-LFSR structures with their feedback defined by reducible characteristic polynomials have proved applicability of such registers and their ability to detect, localize and identify both static and delay faults of buses with non-interleaved connections. The approach that was suggested in (Hławiczka *et al*., 2008a, b) uses the method referred to as identification of a finite state machine. The studies assume that a fault-free R-LFSR register (with the set of faults $F_0 = \varnothing$) with its length of $2n$ is represented by means of the MF_0 graph whereas each physical defect $f_i \in F_j$, (where: i=1,2,..., u; j=1, 2, ..., w; u is the number of all single faults that are taken into account whereas w represents the number of all presumably possible single and multiple faults) transforms the MF_0 graph into another graph denoted as MF_i, where $MF_i \neq MF_0$.

Detection of a fault within the connecting bus requires that for the randomly selected initial state SD the final state (signature) of the sequence S_mF_0 comprising states associated with the fault-free bus and for the series of m subsequent states of that register should be different from every final state (signature) S_mF_j of the sequence that can be obtained when the connecting bus is faulty. In other words, a fault-free R-LFSR initially seeded to the state SD produces the sequence of states S_1F_0, S_2F_0, ..., S_mF_0 during m subsequent clock cycles, which results from the MF_0 graph. On the contrary, any F_j fault of a bus line that is simultaneously a feedback line of the R-LFSR leads to another sequence of states produced by the register, namely SD, S_1F_j, S_2F_j, ..., S_mF_j that is associated with the graph $MF_j \neq MF_0$.

For practical purposes one has to find out the S_mF_0 signature that corresponds to the fault-free interconnecting bus (fault-free R-LFSR) and, on the other hand, the set of signatures $\{S_mF_j\}$ must be determined as well, where every

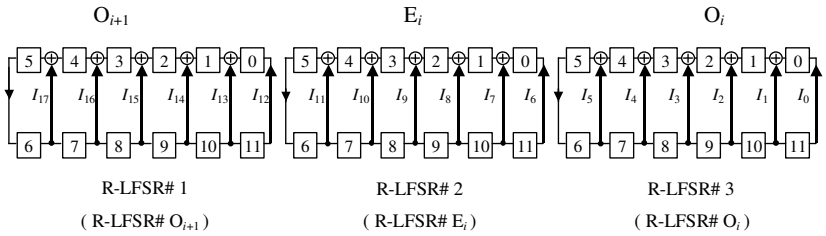

Fig. 1. The IBIST structure: three separated 12-bit R-LFSRs

signature of that set presents the signature that corresponds to a fault that can be modelled on the bus of connections that are simultaneously considered as feedback lines of the R-LFSR. In that way the signature-based diagnostic dictionary $DD = S_mF_0 \cup \{S_mF_j\}$ is obtained. That dictionary enables to detect all those F_j defects that may occur in the interconnecting bus and that meet the condition $S_mF_j \neq S_mF_0$.

Previous experiences of authors (Hławiczka *et al*., 2008a, b) prove that any $2n$-bit ring register (R-LFSR), with $2n \geq 24$ and with feedback lines defined by a reducible characteristic polynomial is capable to produce a test sequence that guarantees detection of all the modelled faults provided that $m \geq n$ and despite the initial seed of the register. The authors of the mentioned studies have also noticed that the modelled faults are highly distinguishable for $m \geq n$ and $n >> 16$, in spite of the randomly selected initial state (seed) of the R-LFSR.

All the aforementioned methods that use an R-LFSR and the associated signature-based diagnostic dictionary suffer from one substantial disadvantage, namely the dictionary volume rapidly increases in pace with the number of n lines that make up the bus under test as well as in pace with the multiplicity of considered faults. For instance, if the n-bit bus comprises hundreds of lines and the fault multiplicity $r \geq 3$ then the fault dictionary size that is directly proportional to the number n^r becomes so huge that the dictionary-based test methods are useless due to practical reasons. In addition, memory volume that is to be occupied by such a dictionary also depends on lengths of signatures that are stored therein. It is why practical applicability of the method that is described in (Hławiczka *et al*., 2008a, b) is limited to buses with their width not more than 32 bits and static faults with the multiplicity factors $r \leq 3$.

The foregoing problem has been partly resolved in (Garbolino *et al.*, 2010a) where the n-bit bus was split into smaller fragments with their width of k bits each (where $n >> k$). These fragments are subjected to simultaneous tests with use of $b = n/k$ mutually separated R-LFSR registers where every register is made up of $2k$ flip-flops. The example of such a solution is presented in Fig. 1 for $n = 18$, $k = 6$ and $b = 3$. The interconnections that are incorporated into the bus under test are marked in the drawing by means of heavy lines and denoted respectively as I_0-I_{17}. When the test operation is to be carried out the bus is split into $b = 3$ mutually separated fragments where each fragment comprises $k = 6$ lines. The test procedure that is applied to each of these fragments employs identical R-LFSRs with the length of $2k$ where each of the $2k = 12$ flip-flops is actually the D-type flip-flop. When the test is in progress all these registers are mutually separated from each other.

It was assumed that the $2k$-bit registers denoted as R-LFSR#1, R-LFSR#2 and R-LFSR#3 are initially seeded with the identical content *SD* with the length of $2k$ bits. Such an assumption makes it possible to use the same diagnostic dictionary for each of these three registers and it also enables to use the test sequence of same length for all the registers, i.e. m clock periods. Let us also assume that signatures obtained for R-LFSR#1, R-LFSR#2 and R-LFSR#3 registers after m clock cycles shall be respectively denoted as S_m*#1,* S_m*#2* and S_m*#3*.

Let us make the constraint that the set of faults that shall be considered in the further part of this study is limited to the following types: AND/OR type shorts between not more than p_{max} adjacent lines, stuck-at-1/0 (Sa1/0) faults as well as delay faults that lead to excessive delays of both the rising and falling edges of transmitted signals. Due to technological reasons the assumption could be made that AND type shorts shall never occur simultaneously with OR type ones. The maximum multiplicity of faults that may occur within each k-bit bus fragment under test was presumed not to exceed r_{max}=3.

Elementary faults that may happen to individual lines of the bus under test are denoted as f_i, where i=1, 2, ...u. Consequently, $F_j = \{ f_{i1}, f_{i2}, ...\}$ stands for sets of such elementary faults f_i that may represent both single as multiple faults within the R-LFSR, where $j = 1, 2, ..., w$.

Cardinality for each of such sets meets the condition $1 \leq |F_j| \leq r_{max}$. Moreover, the set F_0=∅ stands for the case when the bus is free of any faults.

The $2k$-bit signature that is associated with the fault represented by the F_j set shall be denoted as S_mF_j. Therefore *DD* shall stand for the diagnostic dictionary that comprises these $2k$-bit signatures S_mF_j.

Use of identical $2k$-bit R-LFSR registers makes it possible to apply the same diagnostic dictionary (*DD*) to examine each k-bit-wide fragment of the interconnecting bus under test by means of b identical R-LFSR registers. As very wide buses are split into narrow k-bit fragments, even interconnecting buses with their *width* of hundreds lines and suffering from faults with the multiplicity much exceeding the factor that is quoted in (Hławiczka *et al*., 2008a, b) can be tested with the signature-based fault dictionary with its size that is acceptable in practical terms. For instance, the size of the diagnostic dictionary (*DD*) that is to be used to test each k-bit-wide fragment of the bus by means of the same R-LFSR