A FPGA-Based Bit-Word PLC CPUs Development Platform

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Abstract: The conception of the hardware-software platform is presented in the paper. Presented platform is designed in order to test different constructions of the central processing units dedicated to programmable logic controllers. Selected hardware solutions for the PLC dual processor bit-byte (word) CPUs, which are oriented for optimised maximum utilization of capabilities of the two-processor architecture of the CPU are presented in the paper. The key point is preserving high speed of instruction processing by the bit-processor, and high speed and functionality of the byte (word)-processor. The structure should enable the processors to work in concurrent mode as far as it is possible, and minimize the situations, when one processor has to wait for the other. Designed platform is based on the development board equipped with Xilinx Virtex-4 FPGA. Software tool for testing possibilities of the selected units and testing utilization of the programmable structure was also developed.

Keywords: Programmable Logic Controller; Central Processing Unit; Bit-Byte (Word) Structure of CPU; Scan Time, Throughput Time, Concurrent Operation, Field Programmable Gate Array.

1. INTRODUCTION

Entire operation cycle of a PLC (*Programmable Logic Controller*) consists of the following items: network communication, CPU test, object signal update and control program execution. Operations connected with object signal update and control program execution are considered in this paper. There are two typical architectures of a CPU known from literature that can be used. Those are: typical or slightly modified microcontroller (e.g. dedicated processors designed as ASICs - *Application Specific Integrated Circuit* or FPGA – *Field Programmable Gate Array*) and dual processor bit – byte (word) architecture with separated processing of instructions operating on binary and word data. There also exist very expensive multiprocessor solutions.

Generally, computational possibility of the logic controller is defined as a time to execute thousand instructions (Getko, 1983; Modicon, 1990; Michel, 1990). The shorter time of instruction execution, the wider range of the applications that use logic controller. This is especially important for applications, which time constraints are high. Modern industrial objects require more and more complicated control devices. Of course this implies the need of applying control devices that enable of implementation of huge algorithms. Moreover, the implemented algorithm must be executed as fast as possible. The problem of developing of the central processing unit, which execute program in time as short as possibly, is still open (Donandt, 1989; Aramaki at al., 1997; Chmiel and Hrynkiewicz, 2005; Chmiel et al., 2005). This problem gained new platform for efficient and comfortable construct of the fast control units. This platform is based on the programmable logic devices (PLD), especially FPGAs. PLDs develop very dynamically. Designers have powerful tools which ensure acceptable financial and time outlays. PLDs enable easy prototyping and testing solutions on two stages: simulation and implementation.

Besides the instruction execution time, very important parameter (or characteristic feature) is access time to internal resources: markers, counters, timers, and to external resources: inputs and outputs. Another parameter which characterizes PLC is throughput time defined as a response time on the change of the object signals. From the point of view of the object, this parameter is most important (Chmiel, 2008).

All those parameters: the execution of thousand instructions, access time and throughput time are inextricably linked with each other. These parameters depend on each other and arise on each other. While working on the optimization of PLC central processing unit, all defined above parameters must be taken into account.

Is must be noticed, that processes for which PLCs are applied have most of all binary character (strictly digital) or binary with small analogue component. Besides, there are also objects where analogue and digital parts are independent. This observation carry out to conclusion: it is possible to develop central processing units that in literature are called bit-byte (bit-word) – units with two processors for digital and analogue tasks. This structure is oftentimes optimized on very fast logic operations and on execution of the complicated arithmetic expressions. However, to make this possible, two processors must be equipped with specific hardware and software solutions. Firs of all both processors must work as independent as possible. This system must exploit

possibilities of the byte (word) processor and speed of the bit processor.

Conceptions of few central processing units were developed as the effect of research work and theoretical deliberations. These conceptions were simulated and implemented in order to test ideas and compare obtained results with results presented in literature and with units, which offer commercial companies. Preliminary tests were performed.

Authors decided to use development board with Xilinx Virtex-4 (Xilinx, 2006) to perform tests. Logic resources of the Virtex-4 are sufficient to test both standard processors (IP cores) described using hardware description languages, and dedicated processors. It must be mentioned that implemented central processing units work in classical manner – central processing unit executes instruction after instruction (serial-cyclic) in opposite to parallel specific hardware processing which is characteristic for programmable logic devices.

2. FPGA BASIC ACPECTS

Designers have currently possibilities to use programmable structures. One of the most interesting groups of this kind of devices is FPGAs. FPGAs have large amount of logic resources and are integrated circuit designed to be configured by the customer or designer after manufacturing – field programmable, which make them ideal for prototyping. One of the representatives of the FPGA is chosen Virtex-4 (Xilinx, 2008).

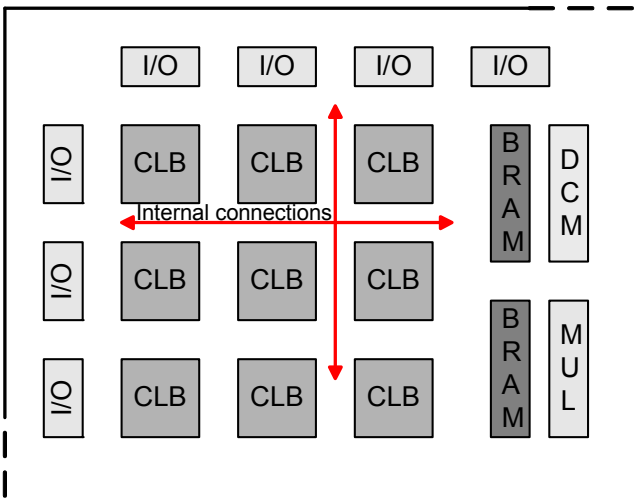

Fig. 1. FPGA block diagram.

The characteristic feature of the field programmable gate arrays is symmetric architecture consisted of matrix of configuration logic blocks (CLB) and the net of horizontal and vertical connections, and input-output blocks surrounded the chip (Fig. 1). Connections are also configured.

Every CLB consists of few elements: look up tables (LUT), flip-flops, multiplexers, internal connections. LUT is called also function generator because the logic is implemented in it. Nets and multiplexers enable for example signal path creation.

I/O blocks enable to connect peripheral devices. Of course I/O blocks have the ability of cooperation in different logic standards.

To increase functionality of the FPGA an extra resources are build in: block RAM, digital clock management (DCM), multipliers. Block RAM is a specific RAM which enables building several types of memory interfaces. DCMs enable configuration and distributing clock signal, while multipliers enable hardware multiplication of arguments (up to 18x18 bits).

As it was said experiments were carried out using Virtex-4 development board (Xilinx, 2006). The development board is equipped with static RAM, Flash memory, RS-232 interface, LEDs, switches, apart from Virtex-4. These resources are sufficient to build simple interface.

Generally, in process of defining the structure hardware description language (HDL) is used. Two languages are used most of all: VHDL, Verilog. A circuit can be described at many levels using HDLs: logic expressions, register-transfer level, up to behavioural. Different model can be build using FPGAs and HDLs. Parallelism is an immanent trait of programmable logic devices, so digital systems which work in parallel can be built. Therefore multiprocessors systems, operating in concurrent way can be implemented in programmable device. Authors used VHDL to develop processors and whole systems based on those processors. Those systems were also provided with specific peripheral blocks.

3. CENTRAL PROCESSING UNITS FOR PROGRAMMABLE LOGIC CONTROLLERS

Bit-byte (bit-word) central processing units are applied in PLCs for a long time. Commercial constructions of bit-byte units are hardly presented in the literature in details. However, the methods of using or two processors cooperating, one for binary processing and one for numeric processing, are presented in the literature. Few ideas of bit-byte units are presented in next subsections.

3.1 Bit-processor as a co-processor

The basic dual processor architecture presented by Aramaki et al. (1997) can use a bit-processor as a kind of co-processor for specific operations. When both processor units are equally privileged, then additional arbitration circuitry is required. The circuit initially decodes an instruction and directs it to the proper processing unit.

3.2 Bit-byte CPU with serial program realisation

A dual-processor architecture presented by Getko (1983) is show in Fig.2, where the instruction decoder selects a processing unit for the execution of the current instruction. When instruction processing is completed, the active processor increments the instruction counter and the cycle starts over. The instruction decoder is usually a part of the bit processor. The instructions processing is deterministic and