
# SEU Emulation in Industrial SoCs combining Microprocessor and FPGA

Igor Villalta , Unai Bidarte , Julen Gómez-Cornejo , Jaime Jiménez , Jesús Lázaro

PII: S0951-8320(16)30944-9
DOI: 10.1016/j.ress.2017.09.028
Reference: RESS 5966

To appear in: *Reliability Engineering and System Safety*

Received date: 13 December 2016
Revised date: 15 September 2017
Accepted date: 30 September 2017

Please cite this article as: Igor Villalta , Unai Bidarte , Julen Gómez-Cornejo , Jaime Jiménez , Jesús Lázaro , SEU Emulation in Industrial SoCs combining Microprocessor and FPGA, *Reliability Engineering and System Safety* (2017), doi: 10.1016/j.ress.2017.09.028

Highlights

- An exhaustive analysis on the different stages of bitstream-based SEU emulation in FPGAs
- A universal solution is proposed for FPGA SoCs, which can be implemented in any board
- High-speed fault injection controlled by an in-chip hard processor
- High-performance BIST-based verification for fault detection
- Tests performed on a real industrial platform