THE INFLUENCE OF THE LOGIC MINIMIZATION ON THE COMPLEXITY OF CIRCUITS REALIZED AS A PART OF GATE ARRAYS AND CUSTOM VLSI

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Abstract: The influence of various procedures of Boolean function system minimization on the complexity of regular circuits of programmable logic arrays and irregular circuits that are synthesized in the design library of Gate Array, is investigated experimentally. *Copyright © 2006 IFAC*

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1. INTRODUCTION

At present, regular array structures of Programmable Logic Arrays (PLA) type are frequently used for realization of control logic of custom Very Large Scale Integration (VLSI). The structures of PLA type realize systems of disjunctive normal forms (DNF) of Boolean functions. These are usually minimized two-level AND/OR representations of systems of functions, as PLA area minimization is reduced to minimization of systems of completely defined Boolean functions in DNF class (Zakrevskij, 1981), which is widely known in design practice. Another way of control block realization is the use of multilevel representations of function systems. Such representations are realized in custom VLSI by irregular multilevel logic circuits in logical gate basis, i.e. in design library. The problem of logic circuits synthesis in the library basis also includes the synthesis of semicustom VLSI in Gate Arrays (GA) (Bibilo, 2002).

The goal of the paper is experimental research of the effectiveness of different logic minimization programmes for circuit synthesis in PLA and GA bases. In the process of GA circuits synthesis, the logic minimization serves as a preliminary stage, i.e. GA circuit synthesis starts with minimized representations of function systems.

2. PLA AND ITS AREA

PLA realizes the system of DNF Boolean functions. For example, the system of Boolean functions

$$
\begin{aligned}
&y_0 = x_0\bar{x}_1x_2x_3 \vee \bar{x}_0x_2x_3 \vee \bar{x}_0x_1x_2 \vee x_0\bar{x}_2x_3 \vee x_0x_1x_2\bar{x}_3;\\
&y_1 = \bar{x}_0x_1\bar{x}_2 \vee x_0x_1x_3 \vee x_0\bar{x}_2x_3 \vee \bar{x}_0x_2x_3;\\
&y_2 = x_0\bar{x}_1\bar{x}_2\bar{x}_3 \vee x_0\bar{x}_1\bar{x}_2x_3 \vee \bar{x}_0\bar{x}_1x_2 \vee \qquad (1)\\
&\vee \bar{x}_0x_2x_3 \vee x_0x_1\bar{x}_2x_3 \vee x_0x_1x_2\bar{x}_3;\\
&y_3 = x_1x_3 \vee x_0x_2x_3 \vee x_0\bar{x}_1x_2x_3 \vee \bar{x}_0x_2x_3 \vee x_0x_1x_2\bar{x}_3;
\end{aligned}
$$

is realized in PLA (fig. 1), which has 4 inputs, 4 outputs and 11 intermediate wires. Each elementary conjunction is realized on one PLA interim wire.

The area S_{PLA} is calculated by the formula:

$$S_{PLA} = (2n + m) \times k \quad \text{(informational cells)}, \qquad (2)$$

where n is the number of inputs of PLA circuit, m is the number of outputs, k is the number of interim wires (the number of elementary conjunctions in the implemented DNF system of Boolean functions).

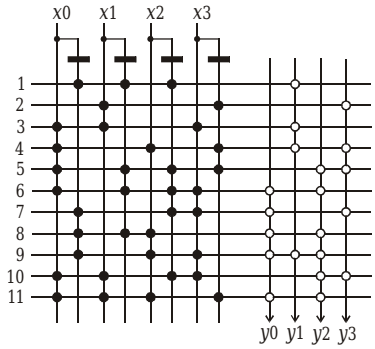

Fig. 1. PLA

The area of PLA circuit shown in fig.1 is 132 (informational cells). The work (Bibilo, 1998) illustrates that formula (2) reflects the actual PLA area well enough, as the value of the chip area for "framing" can be disregarded.

3. THE COMPLEXITY OF GA CIRCUIT

The complexity of circuit S_{GA} in GA design library (henceforth referred to as GA circuit) can be calculated as the sum of the areas of the elements included in the given circuit, and an element's area will be calculated as the number of low-level cells of GA. The area of intercircuit connection of the circuit's elements is not taken into account. Synthesizers of GA logic circuits allow one to calculate the total area of all circuit's elements. The total area of the circuit can be obtained after completion of a laborious stage of the topological design. It has been discovered in the design practice that minimization of the total area of all circuit's elements in the general case leads to the less total area of the array (relevant to elements and intercircuit connections) (Faizulayeva, 1989).

For example, the function system (1) is realized by a logic circuit (fig.2) which is placed in GA. The functions of the logical elements from GA design library, their areas and delays are given in table 1. The area S_{GA} of the circuit (fig.1) is S_{GA} = 67 (elementary GA cells).

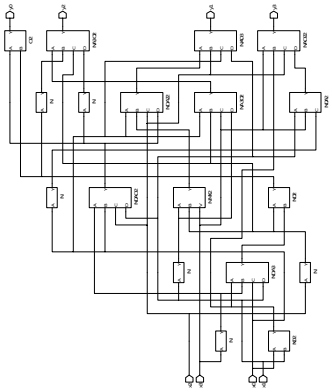
Fig. 2. Logic circuit of elements from GA library.

Table 1 Elements of GA library

Element	Function	Com-plexity	Element's own delay LIB_ EXACT, ps	Element's own delay LIB_ APPROX, ns
N	$Y = \overline{A}$	2	160	0,1
NA3O2	$Y = \overline{AB(C \vee D)}$	5	441	0,3
NAO3	$Y = \overline{A(B \vee C \vee D)}$	5	1000	0,3
NMX2	$y = \overline{(A \vee \overline{V})(B \vee V)}$	6	593	1,0
NO2	$y = \overline{A \vee B}$	3	299	0,2
NO3A2	$y = \overline{A \vee B \vee DC}$	5	643	0,3
NOA2	$y = \overline{A \vee BC}$	4	346	0,2
NOA22	$y = \overline{AB \vee CD}$	5	477	0,2
NOA3	$y = \overline{A \vee BCD}$	5	570	0,3
NOAO2	$y = \overline{A \vee B(C \vee D)}$	5	570	0,2
O2	$y = A \vee B$	4	601	1,0

4. THE PROGRAMMES OF LOGIC MINIMIZATION

Programme 1 of joint minimization of Boolean function systems in DNF class. The programme is described in (Toropov, 1999).

Programme 2 of joint minimization of Boolean function systems in DNF class is based on the algorithm described below.

The optimization criterion in programmes 1, 2 is the number $k_{\min}$ of the common elementary conjunctions on which the minimized DNFs of the functions of the system are given. Programmes 1, 2 allow one to minimize the PLA area which is calculated by the formula (2).

A 3-step algorithm is implemented in programme 2.

Step 1. The search for all prime implicants of the input DNF system of Boolean functions.
Step 2. Constructing the cover matrix A and its reduction.
Step 3. The search for the minimum column covering of matrix A.

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