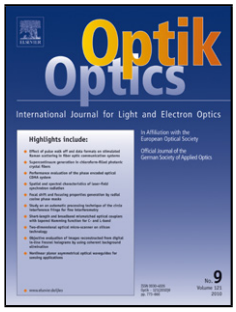

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Designing a 2-to-4 decoder on Nano-scale based on quantum-dot cellular automata for energy dissipation improving

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Abstract

Rapid progress in very large scale integration (VLSI) technology is the main step for having a reliable design with low power consumption. The quantum dot cellular automata (QCA) can be such an architecture at Nano-scale and is developed as a feasible alternative for the current complementary metal–oxide–semiconductor (CMOS) designs. The decoder in the QCA is a very important circuit to address the QCA-based random access memory arrays. They play a key role in many circuit designs, such as field programmable gate array (FPGA), controlled logic block (CLB) and memory circuits designs. Therefore, this paper offers a modular design methodology to build a 2-to-4 decoder in QCA using five-input majority gate. The proposed 2-to-4 QCA-based decoder can be utilized to synthesize n-to-2^n decoders. The functional correctness of the proposed circuit is evaluated using QCADesigner tool. Also, QCAPro simulator as a popular power estimator tool in QCA evaluates the power dissipation. The obtained results show significant achievement in terms of clock speed (%57), wire-crossing (%33), cell number (%27), area (%26) and power dissipation lesser than existing designs.

Keywords: Quantum dot cellular automata, power consumption, decoder, Nanoscale, QCA.

1. Introduction

Lent [1] has introduced Quantum-dot Cellular Automata (QCA) in 1993 [1]. It requires low power and high density and regularity. Also, it is advocated as new device architectures for nanotechnology [2]. Cells are made up of four quantum dots along corners of a square with two free electrons. The two possible arrangements represent logic 0 or logic 1 [3, 4]. The state of the cell is determined by the Columbic interactions with neighboring cell states [4, 5]. Circuits occupy smaller area using QCA technology compared to complementary metal-oxide-semiconductor (CMOS). Thus, they stand as a good alternative to the CMOS technology [6]. The power consumption is considerably lower than conventional CMOS circuits because of electrical current absence in QCA computations. However, many QCA logical and arithmetic designs have completely ignored the power consumption issue of the circuits [7].

On the other hands, the decoder is a circuit that modifies a code into a set of signals. The line decoder is considered as a type of decoder, which receipts an *n*-digit binary number and decodes it into *2n* data lines. The simplest decoder is the 1-to-2. Larger line decoders can be designed in a similar fashion, but just like other digital circuits, smaller decoders combine together for making large decoders. An alternate circuit for the 2-to-4 line decoder which is changing the 1-to-2 decoders with their circuits will show that both circuits are equivalent. In a similar fashion, a 3-to-8 decoder can be designed based on 1-to-2 and 2-to-4 decoders, and a 4-to-16 decoder can be