Journal of Electrostatics 67 (2009) 263–266

Contents lists available at ScienceDirect

Journal of Electrostatics

journal homepage: www.elsevier.com/locate/elstat

Induction charging risk assessment: Charged board alike discharges to metal and human body

Lars Fast [a,*], Jaakko Paasi [b], Jeremy Smallwood [c], Ingvar Karlson [a]

[a] SP Technical Research Institute of Sweden - Electronics, P.O. Box 857, SE-50115 Borås, Sweden
[b] VTT Technical Research Centre of Finland, P.O. Box 1300, FI-33101 Tampere, Finland
[c] Electrostatic Solutions Ltd., 13 Redhill Crescent, Bassett, Southampton, SO16 7BQ, UK

ARTICLE INFO

Article history:
Received 15 September 2008
Received in revised form
14 November 2008
Accepted 15 January 2009
Available online 5 February 2009

Keywords:
Risk assessment
Electrostatic discharge
ESD sensitive devices

ABSTRACT

Charge can easily be induced on electronics or on other conducting parts if they are exposed to external electrical fields. In production facilities where sensitive electronics are handled, strong electrostatic fields should be avoided due to the risk of causing electrostatic discharges (ESDs) that could damage components. In electronics manufacturing this is usually achieved by grounding all conductors and removing all insulators from an ESD Protected Area (EPA) in the facility. However, it is not always possible to remove all insulators from the EPA as they are sometimes an essential part of the production processes. In this case, a method of risk assessment is necessary to evaluate safe operation. We have studied induction charging of a dummy PWB (Printed Wiring Board) through a grounded MOSFET transistor, by grounding it directly to metal or through the human body, when the PWB is exposed to a static electric field. The experimental setup can easily be turned into an induction charging probe by changing the MOSFET transistor to a low leakage current, high voltage capacitor of suitable size and measuring the voltage over this capacitor.

1. Introduction

In an electrostatic discharge (ESD) Protected Area (EPA) all process essential insulators which cannot be removed from the EPA should be assessed with respect to the risk of generating strong electrostatic fields and ESD. To evaluate the risk due to electrostatic fields it is necessary to measure the field or potential and to compare it with the sensitivity of the components and devices that are handled in the area. In international standards for the protection of electronic devices from electrostatic phenomena, there are requirements that ESD sensitive devices (ESDS) should not be exposed to electrostatic fields exceeding 10 kV/m or, alternatively, if the potential exceeds 2000 V the distance from ESDS to the charged object should be more than 30 cm [1,2]. The susceptibility of devices to ESD is usually measured for an ESD test model simulating a specific type of ESD source, either according to the Human Body Model (HBM), the Machine Model (MM) or the Charge Device Model (CDM) [1–3]. If the field or the potential is sufficiently low at a specific point where the device is handled one could assume that it should be quite safe to handle the device at this point. If the field or the potential is high at this point it might not be safe to handle the device there. However the question remains, at what threshold level does the field really start to pose an ESD damage risk to the component?

If ESD withstand voltage levels have been measured using one or more of the device test models, it might be possible to interpret these results as induced charge on the component and to associate the withstand voltage to this induced charge. If this correlation is possible, then it may be possible to evaluate ESD risk as induced charge on a dummy device instead. This paper presents measurements of the breakdown voltage of a specific component, the MOSFET 2N7000. The damage threshold voltage was determined not by using the conventional MM, HBM or CDM, but by using a metal plate as the component holder and exposing this metal plate to a known and well defined electrical field. This would correspond to a charged board model (CBM) discharge [4–6] for a PWB (Printed Wiring Board) defined by us. To initiate ESD, the device was grounded either directly or indirectly through the human body, whilst the device and the plate were exposed to the field.

In this paper we have studied simulated electrostatic field induced CBM, showing also how the test arrangement can be transformed into a field probe for risk analysis. In [7], CBM was studied with a similar technique, using a slightly different experimental setup and only grounding the component directly.

* Corresponding author. Tel.: +46 10 516 5402; fax: +46 33 121930.
E-mail address: lars.fast@sp.se (L. Fast).

0304-3886/$ – see front matter © 2009 Elsevier B.V. All rights reserved.
doi:10.1016/j.elstat.2009.01.024

2. Description of the experiment

A simple design of the experiment was chosen in order to make modelling of system easy and to make the transformation of the experimental setup into a charge induction probe possible. The experimental setup consisted of a layered structure. A charged plate, with the radius 15 cm was kept 5 cm from the grounded plate, which was essentially 4 times larger in area than the charged plate (Fig. 1). A PWB of radius 7.5 cm was placed a further 5 cm from the charged plate, with the device under test (DUT), in this case a MOSFET transistor, mounted centrally on it (on the side facing away from the charged plate). The drain and the source of the transistor were soldered together and connected to the PWB. All three plates were thin, flat and kept parallel to each other. The distance to ground, other than to the ground plate, was large compared to the size of the three plates. The potential of the charged plate (U_{plate}) could be varied and the potential of the PWB (U_{PWB}) measured with the aid of a non-contact electrostatic voltmeter, which was fastened in a plastic insulator (∅ = 1.5 cm, L = 2.5 cm) glued to the centre of the PWD. The voltmeter was held by a grounded metal rig (mimicking a hand). The effect of the plastic insulator is negligible, because of the small size. The experiments were performed in a controlled environment, 12% RH and 23 °C.

The potential of the charged plate and the potential of the PWB were measured before the DUT was grounded. The potential of the PWB was also measured after the PWB was grounded. If the potential of the PWB suddenly dropped (close to zero), after the grounding of the board, as function of increasing potential for the charged plate, then it was assumed that the component might be damaged and should be checked properly. It was essential to discharge the PWB and the DUT in zero field after every time the component was grounded, because of leakage current through the DUT. It is important to be careful when analysing the results, so that the operator capacitance is taken into account. The effect of this is indicated by a non-zero, but low, potential when the DUT has a short circuit. All voltmeter readings were taken with operator far away from the experimental setup, however when the operator grounded the component, he, and especially with his hand, was very close to the experimental setup. The ground connection was only kept for a short time.

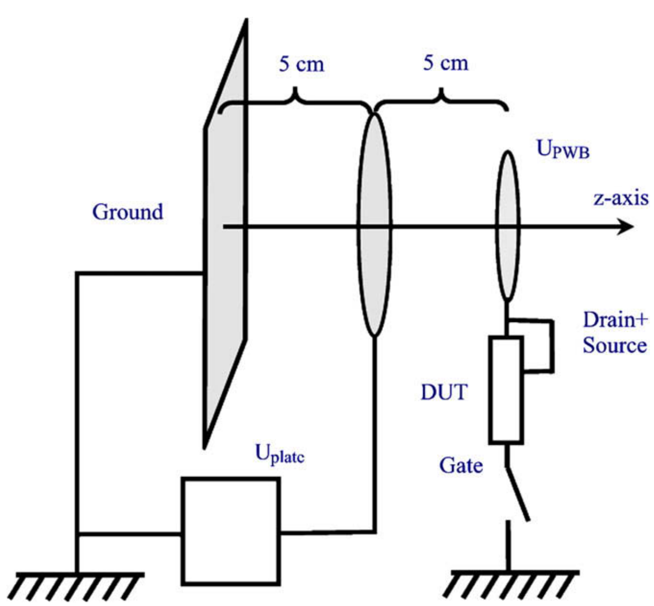

Fig. 1. Experimental setup of the CBM component tester. From left to right, are shown the ground plate, the charged plate and the PWB. The DUT is connected to the centre of the PWB. The potential of the charged plate (U_{plate}) is controlled and the potential of the PWB (U_{PWB}) is measured with a non-contact voltmeter. The switch indicates that the DUT can be grounded.

In order to check the component status after exposing it to a CBM discharge, the gate-source resistance was measured according to reference [8].

3. Description of the model

The experimental setup was modelled in the same way as in reference [9]. It followed the arrangement of Fig. 1, except that the charge density on the charged plate and on the PWB, were assumed to be constant, but different. This, in practice, was not true in our experiment where the charge densities, around the edges were different, from at the centre. For simplicity, the potential was only calculated along the z-axis. The simplest form of the model is presented in equation (1) below.

$$V(z) = \frac{\sigma}{2\varepsilon_0}\left\{\sqrt{(z-d)^2+R^2} - |z-d| - \sqrt{(z+d)^2+R^2} + |z+d|\right\} - \frac{\sigma_I}{2\varepsilon_0}\left\{\sqrt{(z-d_I)^2+R_I^2} - |z-d_I| - \sqrt{(z+d_I)^2+R_I^2} + |z+d_I|\right\} \quad (1)$$

where (σ) is the charge density of the charged plate and (σ_I) is the charge density of PWB. The distance from the ground plane to the charged plate is denoted (d) and was 5 cm and the distance from the ground plane to the PWB is denoted (d_I) and was 10 cm. The radius of the charged plate is ($R = 15$ cm) and the radius of the PWB is ($R_I = 7.5$ cm). The ground plane is assumed to be infinite and is modelled as a mirror plane. Since both the charged plate and the PWB are round and are assumed to have constant charge densities, the amount of charge on each plate could easily be calculated. Typical capacitance of the DUT was 48 pF (with drain and source were connected together), with gate breakdown voltage of around 70 V [4] and that the potential of the charged plate is controlled in the experiment. Combining this information with equation (1) it is possible to make a theoretical calculation for the model system.

4. Results

We exposed 20 MOSFET transistors to the static electric field defined by the experimental setup in Fig. 1 using a controlled potential applied to the charged plate. The potential on the charged plate and on the PWB were recorded before and after the grounding of the DUT. Ten of the transistors were grounded directly and the remaining 10 transistors were grounded via the operator's body.

For the case when the transistors were grounded directly, Fig. 2(a) shows the voltages before grounding the transistor, and Fig. 2(b), after grounding the transistor. In both Fig. 2 (a) and (b) the potential of the PWB is shown as function of the applied potential on the charged plate. The model calculations were made assuming that there was zero charge on the PWB. In both figures there is reasonable agreement between experimental results and the model calculation. We used the component capacitance of around 48 pF and the potential of the charged board to calculate the potential of the PWB. The breakdown voltage of the transistor is not indicated in the diagram, since we only know that is was around 70 V.

For the case when the transistors were grounded through the operator's body, the results are presented in Fig. 3(a) (before