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Design of on-chip 15~18 GHz ultra low noise amplifier

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Abstract

With rapid development communication system, high signal to noise ratio (SNR) system is required. In high frequency bandwidth, high loss, low Q inductors and high noise figure is a significant challenge with on-chip monolithic microwave integrated circuits (MMICs). To overcome this problem, high *Q*, low loss transmission line characteristics was analyzed. Compared with the same inductor value of the lumped component and the transmission line, it has a higher *Q* value and lower loss performance in high frequency, and a 2-stage common-source low noise amplifier (LNA) was presented, which employs source inductor feedback technology and high *Q* low loss transmission line matching network technique with over 17.6 dB small signal gain and 1.1 dB noise figure in 15 GHz–18 GHz. The LNA was fabricated by WIN semiconductors company 0.15 μm gallium arsenide (GaAs) *P* high electron mobility transistor (P-HEMT) process. The total current is 15 mA, while the DC power consumption is only 45 mW.

Keywords LNA, GAAS P-HEMT, MMIC, *K*-bAND

1 Introduction

With rapid development of electronic information, the radio frequency (RF) front-end requirement is higher than expected. With critical requirement of information, low noise, high reliably and low consumption devices are required. Low noise amplifiers are adapted in a wide variety of applications in the RF communication systems, such as wireless computer networks, mobile phones and satellite receivers. In fact, the function of LNA is to amplify a very weak signal which received from an antenna, while restraining added as little noise as possible. The complementary metal oxide semiconductor (CMOS) LNA is, indeed, easy to be integrated. Much work was reported [1–4]. Meanwhile, in order to achieve low noise, high gain and good temperature characterizes, the HEMT device is a good candidate for *K*-band LNA design [5–7], but they usually used lumped inductor as the matching network because of the lumped inductors topology structure, For the Si substrate, the eddy current could be produced under the lumped inductance in high frequency which decrease the *Q* value of the on-chip inductor. This phenomenon can decrease the SNR of the communication system. In this article, by using the high *Q* low loss transmission line instead of lumped inductors as the matching network, small signal gain can be increased and the SNR is improved as well. In 0.15 μm GaAs technique, LNA with the lowest noise characterizes in all reports at the *K*-band frequency bandwidth is presented. Table 1 summarizes reports of *K*-band LNA.

This article refines the *K*-band LNA used source series feedback inductance with 0.15 μm GaAs WIN technology which operates in 15 GHz~18 GHz with high gain, low noise and low power consumption. The technology was introduced in Sect. 2. The two-stage LNA topology and the design method were demonstrated in Sect. 3. In Sect. 4, simulation and discussion is given. Lastly, outline and overall conclusion is described in Sect. 5.

2 Technology

LNA MMIC was implemented in 0.15 μm GaAs P-HEMT MMIC process with 100 μm GaAs substrate with scratch protection by WIN semiconductors. The excellent device level with f_t is about 95 GHz and $f_{\max}$ is about

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150 GHz. A typical device exhibits high transconductance (Gm) with a peak greater than 550 mS/mm and maximum current density over 500 mA/mm. The process is designed to operate with maximum rating of 4 V drain bias and exhibits typical breakdown voltage of 13 V and pinch-off voltage is −0.45 V. Other passive components such as thin-film resistors, metal injection mdding (MIM) capacitors, Spiral inductors and air-bridges are all available.

3 LNA topology and design method

3.1 General considerations

In multistage amplifier design, such as two-stage low noise amplifier in Fig. 1, the overall noise figure (NF) is expressed as follow [8]:

$$F = F_1 + \frac{F_2 - 1}{G_1} \quad (1)$$

F is the total noise figure of LNA. NF_1 is the first stage to produce the noise figure, and NF_2 is the noise figure of the second stage. G_1 is the available gain which belongs to the first stage. Obviously, the equation 1 shows that the first stage is key to the whole LNA's noise figure performance. Therefore, the first stage design should ensure that the LNA has the lowest NF (minimum noise figure matching in first stage). Comparing with the first stage, the second stage aims to supply the whole LNA's enough gain (conjugate matching) to ensure amplifying week signals which is received from antenna.

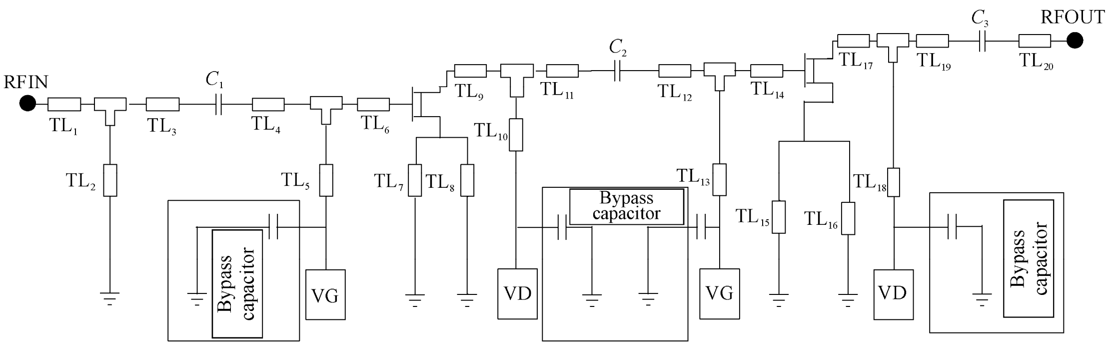

Fig. 1 Schematic of the 2-stage LNA

3.2 Active device choice

To obtain the lowest noise, high gain, good return loss performance and circuit stability, the gate width (W) and gate fingers (N) were simulated with the advanced design system (ADS). The simulation result showed that compared with the large transistor, the smaller transistor with higher gain and smaller noise figure, but which is difficult to tradeoff between input return loss and noise figure. The obtained result was as same as other technology in GaAs P-HEMT [9–10]. Taking the current consumption and stability of device into account, GaAs P-HEMT device (2×25 μm) was chosen under the V_{dd}=3 V and V_{gs}=−0.375 V which was bias condition for the first stage with source inductor feedback, and a single P-HEMT device (2×50 μm) was chosen for the second stage with the same bias condition to achieve the lowest noise figure, low current consumption, good return loss, enough gain and stability.

3.3 Passive device choice

In order to achieve low loss and noise quality properties, the high Q transmission line was selected for this circuit matching design. Compared with the lump component, the distributed component has a higher Q value as shown in Fig. 2 and Fig. 3.

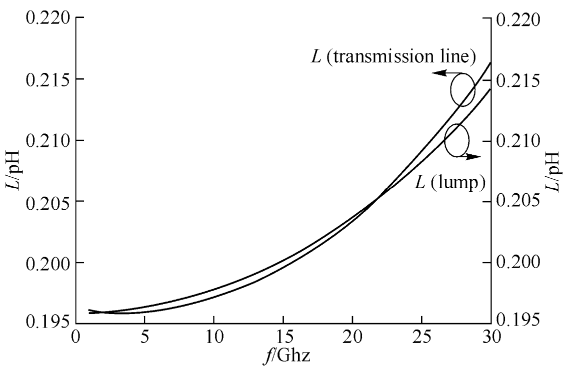

Fig. 2 The L Value