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Novel high-PSRR high-order curvature-compensated bandgap voltage reference

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Abstract

This paper proposes a novel high-power supply rejection ratio (high-PSRR) high-order curvature-compensated CMOS bandgap voltage reference (BGR) in SMIC 0.18 μm CMOS process. Three kinds of current are added to a conventional BGR in order to improve the temperature drift within wider temperature range, which include a piecewise-curvature-corrected current in high temperature range, a piecewise-curvature-corrected current in low temperature range and a proportional-to-absolute-temperature $T^{1.5}$ current. The high-PSRR characteristic of the proposed BGR is achieved by adopting the technique of pre-regulator. Simulation results shows that the temperature coefficient of the proposed BGR with pre-regulator is 8.42×10^{-6}/°C from −55 °C to 125 °C with a 1.8 V power supply voltage. The proposed BGR with pre-regulator achieves PSRR of −123.51 dB, −123.52 dB, −88.5 dB and −50.23 dB at 1 Hz, 100 Hz, 100 kHz and 1 MHz respectively.

Keywords bandgap voltage reference, pre-regulator, temperature coefficient, power supply rejection ratio

1 Introduction

Precise bandgap voltage references (BGRs) are widely used in analog and mixed signal devices [1–3], such as power management [1–2], radio frequency circuit [3], and so on. Conventional BGR inspired by Widlar in Ref. [4] and Brokaw in Ref. [5] is first-order temperature compensation. In fact, the first-order BGR has a relatively high temperature coefficient (TC) because of the nonlinearity of the base-emitter voltage V_{BE} of NPN bipolar transistor. Therefore, the first-order BGR cannot meet the requirement of high precision application.

To improve the temperature coefficient of BGR, many high-order temperature compensation techniques [6–13] have been reported, such as MOS field effect transistor (MOSFET) operation in sub-threshold region [6], resistorless technique [7], curvature compensation technique [8–13], and so on. With regard to modern SoC design, there are many analogue building blocks that were placed on the same chip with noisy digital circuits, switched capacitor and RF circuits, and the analogue building blocks will suffer from noise on power supply lines. Regarding to the other noise, the most significant noise injected to the output of BGR is the supply noise. Therefore, a high-PSRR BGR should be required for high precision applications over broad frequency range to reject supply noise. In the recent past, many approaches have been developed to improve the PSRR of BGR [14–19], such as pre-regulator technique [14], pseudo floating voltage source technique [15], cascade technique [16], low dropout regulator technique [17], supply independent current source technique [18–19], and so on. In general, those reported BGRs with improvement PSRR techniques have a relatively high temperature coefficient. Therefore, the high PSRR and low temperature drift BGR should be still analyzed and designed for the requirements of high precision circuits.

A novel high-PSRR high-order curvature compensation CMOS BGR is proposed in this paper, which is realized by

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adding three kinds of current to a conventional BGR including a piecewise-curvature-corrected current in high temperature range, a piecewise-curvature-corrected current in low temperature range and a proportional-to-absolute-temperature $T^{1.5}$ current. Furthermore, we adopt the technique of pre-regulator to improve the PSRR performance of BGR. Sect. 2 will discuss the conventional BGR. Sect. 3 will discuss the proposed BGR without pre-regulator, while the proposed BGR with pre-regulator will be analyzed in Sect. 4. Simulation results will be given in Sect. 5. Finally, conclusions will be given in Sect. 6.

2 The conventional BGR

Fig. 1 shows the typical implementation of a conventional BGR in CMOS technology consisting of MOSFETs M_1~M_5, resistors R_1~R_3, PNP bipolar transistors Q_1~Q_2 and amplifiers A_1~A_2. Bipolar transistor Q_2 has an emitter are that is m times that of bipolar transistor Q_1. MOSFETs M_1~M_2 and M_4 are entirely the same and MOSFETs M_3 and M_5 are entirely the same. The high-gain amplifier A_1 forces the voltages of nodes A and B to be equal and the high-gain amplifier A_2 forces the voltages of node B and node C to be equal. Therefore, the output voltage V_{REF} of the conventional BGR can be express as:

$$V_{\mathrm{REF}} = \frac{R_3}{R_2}V_{\mathrm{EB1}} + \frac{R_3 \mathrm{k}T}{qR_1}\ln m \tag{1}$$

where k is the Boltzmann's constant, q is the electronic charge, T is the absolute temperature and V_{EB1} is the emitter-base voltage of PNP bipolar transistor Q_1. The second item in Eq. (1) is proportional to the absolute temperature voltage (V_{PTAT}) coming from the thermal voltage ($\mathrm{k}T/q$), which can compensate the negative temperature coefficient of V_{EB1}. In fact, the relationship between V_{EB} of the PNP bipolar transistor and temperature T is a nonlinear which can be expressed as [20]:

$$V_{EB} = a_0 + a_1 T + a_2 T^2 + \cdots + a_n T^n \tag{2}$$

where a_0, a_1, … and a_n are the corresponding coefficients. The first-order temperature-dependence factor of V_{EB1} in Eq. (1) can be compensated by V_{PTAT}, but the high-order temperature-dependence factor cannot be compensated with V_{PTAT} in the conventional BGR. Therefore, the conventional BGR has a high temperature coefficient.

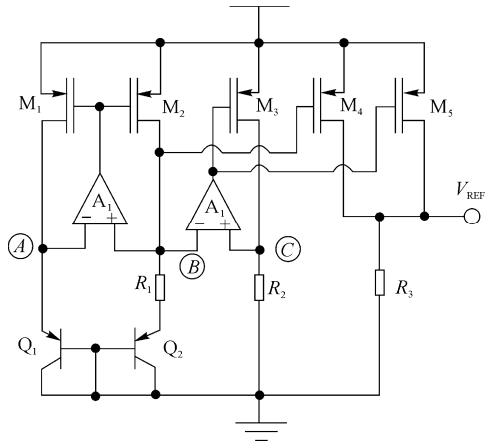

Fig. 1 The conventional BGR in CMOS technology

3 Design and analysis of proposed BGR without pre-regulator

Compared to the conventional BGR shown in Fig. 1, the proposed high-order curvature-compensated BGR shown in Fig. 2 achieves the lower temperature coefficient by adding three kinds of current to the conventional BGR, which includes a piecewise-curvature-corrected current I_{19} in low temperature range, a piecewise-curvature-corrected current I_{35} in high temperature range and a proportional-to-absolute-temperature $T^{1.5}$ current I_{25}.

The proposed high-order curvature-compensated BGR shown in Fig. 2 is made up of MOSFETs M_9~M_{37}, PNP bipolar transistors Q_1~Q_2, resistors R_1~R_3 and amplifiers A_1~A_2. Bipolar transistor Q_2 has an emitter area that is m times that of bipolar transistor Q_1. Amplifiers A_1 and A_2 are entirely the same, and their DC-gain A_{d} has that $A_{\mathrm{d}} >> 1$. The amplifier A_1 forces the voltages of nodes A and B to be equal and the amplifier A_2 forces the voltages of nodes B and C to be equal, i.e. $V_A = V_B = V_C = V_{\mathrm{EB1}}$. Here, V_A, V_B and V_C are the voltage of nodes A, B and C respectively, and V_{EB1} is the emitter-base voltage of bipolar transistor Q_1. For convenience, it is assumed that I_j, W_j and L_j are the drain current, channel width and channel length of MOSFET M_j respectively, here j=9, 10, 11,…, 37. MOSFETs M_9 and M_{10} are entirely the same. So, the drain current I_{10} of MOSFET M_{10} has that $I_{10} = (\mathrm{k}T\ln m)/(qR_1)$ and the drain current I_{11} of transistor M_{11} has that $I_{11} = V_{\mathrm{EB1}}/R_2$. Resistors R_1~R_3 adopt the same material, so R_3/R_1 and R_3/R_2 are almost independent of temperature T. It is concluded that $I_{10}R_3$ is