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Oxide interfacial charge engineering towards normally-off AlN/GaN MOSHEMT

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ABSTRACT

In this paper a detail insight into the role of oxide/barrier interfacial charges (N_{ox}) for shifting the threshold voltage (V_T) of AlN/GaN metal oxide semiconductor high electron mobility transistors (MOSHEMTs) is gained. A model is developed for V_T considering all possible charges arise at different interfaces. To validate the model the proposed device is simulated by considering different insulators and N_{ox} into account. It is very fascinating to observe that V_T is highly sensitive towards change in N_{ox} at higher oxide dimensions, whereas at lower dimensions N_{ox} has very negligible effect. Normally-off operation can be achieved by increasing or decreasing N_{ox} in MOSHEMT with Al_2O_3 or HfO_2 as gate dielectric respectively.

1. Introduction

Inherent high gate leakage current in High Electron Mobility Transistors (HEMTs) not only degrades the device performance in terms of gate voltage swing, power added efficiency and noise [1,2] but also responsible for drain current collapse [3]. In case of MOSHEMT an oxide layer is grown on barrier layer before gate metallization, which not only reduces the gate leakage current but also avoids current collapse and improves on-state drain current performance by nearly 40% [4]. The insulator layer can be SiO_2 [5], HfO_2 [6], Al_2O_3 [7], Ga_2O_3 [8], Si_3N_4 [9], MgO [10], Sc_2O_3 [10] or TiO_2 [11]. Recently AlN/GaN MOSHEMTs have been demonstrating promising performance in high power applications because of high bandgap and polarization property of AlN [12]. It's very substantial that the AlN barrier grown over GaN buffer should be very thin i.e. below critical thickness in order to obtain normally-off operation [13]. This results in lower sheet charge density (n_S), and hence higher sheet resistance (R_S) [14]. Meanwhile, there is an opportunity of achieving positive threshold voltage with lower n_S because at zero gate bias (V_{gs}) the channel is depleted and a positive V_{gs} is required to induce the channel. A positive V_T is obtained by considering sub-critical barrier thickness i.e. only 1.5 nm [15]. For power electronics applications normally-off operation is required to simplify the design of the driving circuit by eliminating the requirement of negative voltage supply and to reduce the switching [16] and off-state standby power loss [17].

In MOSHEMTs, oxide charges formed because of defects generated during oxidation play a vital role in tuning V_T depending on amount and polarity. The amount of N_{ox} depends on the deposition technique adopted during oxidation process [18]. There are many literatures evident regarding the impact of V_{gs} dependent oxide/semiconductor interface trap charges on V_T [18,19]. However study related to the effect of variation in interfacial and bulk oxide charges for different dielectric materials on shift in V_T forms the motivation behind the present work. The remaining of the paper is described as follows. Section 2 describes the device structure, simulation setup and model development. In Section 3 results are discussed. Finally in Section 4 the paper is concluded.

2. Model development for threshold voltage

The structure considered for simulation is similar to that of fabricated in Ref. [20] except AlGaN barrier layer which is replaced by AlN layer as shown in Fig. 1. The gate bias dependent 2-dimensional electron gas (2DEG) at AlN/GaN interface forms the channel between source and drain. The dimensions of different layers of the device are enlisted in Table 1. The gate width is considered to be by default 1 μm in Silvaco TCAD [21]. In this study three oxide layers such as SiO_2, Al_2O_3, and HfO_2 with different dielectric constants and charges have been considered. Similarly the thickness of the oxides also varies from 2 nm to 20 nm during the study.

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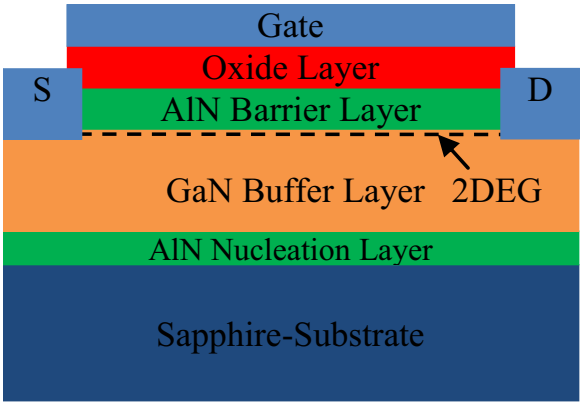

Fig. 1. AlN/GaN MOSHEMT structure.

Table 1
Parameters used for the Simulated Device.

Parameters	Dimensions
Gate Contact Length	6 μm
Source to Drain Distance (Effective Gate Length)	5.5 μm
AlN Barrier Thickness	2 nm
GaN Buffer Thickness	3 μm
AlN Nucleation layer thickness	5 nm
Sapphire Thickness	350 μm

2.1. MOSHEMT structure and dimensions

See Fig. 1 and Table 1.

2.2. Simulation setup

Drift–diffusion numerical model including carrier continuity equation and Poisson equation is used for the simulation of carrier transport in the channel at 300 K. Newton method is used for model calculations. Mesh value of the structure is carefully chosen by the Deck Build Editor for the accurate simulation of the important regions of the device as well as to accelerate the computational efficiency. A fine meshing is done in Deck build Editor around the gate foot and channel region such that there are 60 nodes within 2 nm thick barrier, i.e. distance between two nodes is around 0.6 Å. Simulations have been established using the physical models such as, FLDMOB which accounts for the electric field-dependent mobility, CONMOB, which accounts for the concentration dependent mobility, and CVT-a stand-alone model which incorporates all the effects required for simulating the carrier mobility, Fowler-Nordheim model for gate leakage current, SRH recombination and generation and Auger recombination model. Traps have been modeled by including Shockley–Read–Hall recombination terms in the continuity equation. The results are analysed in Tony plot and for output data extraction the Tony plot export feature is used.

During simulation the fixed oxide charges (V_{gs} independent) at oxide/semiconductor interfaces are considered as follows. N_{ox} is varied from $-4.5\times10^{12}\,cm^{-2}$ to $-9.2\times10^{12}\,cm^{-2}$ for Al_2O_3, $4.9\times10^{12}\,cm^{-2}$ to $9.8\times10^{12}\,cm^{-2}$ for HfO_2 [18] and $-1.6\times10^{12}\,cm^{-2}$ to $-3.2\times10^{12}\,cm^{-2}$ for SiO_2 [22]. As the amount of oxide charges is dependent on deposition technique, for simulation purpose and to maintain uniformity among the oxides, in one case this value is referred from literature and in another case it is doubled. The strain dependent polarization charges of $6.8\times10^{13}\,cm^{-2}$ and $5\times10^{13}\,cm^{-2}$ are calculated and considered across oxide/AlN and AlN/GaN interface respectively [23].

2.3. Model Development for V_T

The schematic representation of conduction energy band across the metal/oxide/barrier/GaN heterojunction along with the charges formed at different interfaces is shown in Fig. 2.

The charge distribution across the junctions is also shown at the bottom of the figure, where σ_1 represents the negative charge due to both spontaneous and piezoelectric polarization at oxide/AlN junction, n_s represents 2DEG density at AlN/GaN interface. The net charge at oxide/AlN junction consists of mainly four charge components such as positive surface donor trap charges (qN_d), negative net polarization charges (σ_1), negative oxide/AlN interfacial charge and fermi level dependent interface charge (due to interface density of state, d_{it}) [24]. Among the above mentioned charges, N_d is always positive because of empty donor traps present at the surface of barrier and these trap states are the source of electrons inside the 2DEG which is still under debate [25]. N_{ox} is negative for SiO_2 and Al_2O_3 but positive for HfO_2 [18]. The polarity of N_{it} in fact depends on the position of fermi energy dependent, so it is determined by gate bias. As most of these charges concentrate at the oxide/barrier interface the effect of bulk oxide charges can be neglected. So the V_T expression for this structure can be written as,

$$V_T = \phi_b - \Delta E_c - \phi_F - \frac{t_{ox}}{\epsilon_{ox}}(\sigma_1+\sigma_2) - \frac{t_b}{\epsilon_b}\sigma_2 - \frac{t_{ox}}{\epsilon_{ox}}q\left(N_d + N_{it}(E_F) + N_{ox}\right) \quad (1)$$

where ϕ_b is the metal to semiconductor barrier height at zero gate bias, ΔE_c is the conduction band offset at oxide/AlN interface, ϕ_F is the GaN bulk fermi potential, σ_2 is the polarization charge (equivalent of spontaneous and piezoelectric polarization charge of AlN and spontaneous polarization charge of GaN) at AlN/GaN interface, t is the thickness, ε is the permittivity, and the subscripts ox and b refer to oxide and barrier respectively, N_d is the surface donor trap charge, $N_{it}(E_F)$ is the oxide/AlN interface trap charge which is a function of E_F as $N_{it}(E_F) = D_{it}.(E_F - E_{NL})$, where E_{NL} is the charge neutrality level present at the center of oxide band gap as shown in Fig. 2. It can be assumed as constant for the same range of V_{gs} when V_T is to be studied with respect to variation in N_{ox}. As

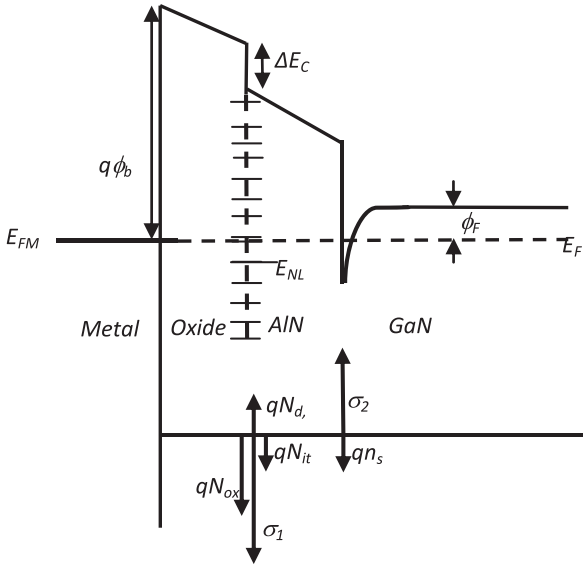

Fig. 2. Conduction band profile along with various charge distribution (bottom) in AlN/GaN MOSHEMT. Upward arrow shows positive charges and downward arrow shows negative charges.